960L

Multi-Channel
Digital Effects System

Service
Manual

Lexicon

Precautions

Save these instructions for later use.

Follow all instructions and warnings marked on the unit.

Always use with the correct line voltage. Refer to the manufacturer's operating instructions for power requirements. Be advised that different operating voltages may require the use of a different line cord and/or attachment plug.

Do not install the unit in an unventilated rack, or directly above heat producing equipment such as power amplifiers. Observe the maximum ambient operating temperature listed in the product specification.

Slots and openings on the case are provided for ventilation; to ensure reliable operation and prevent it from overheating, these openings must not be blocked or covered. Never push objects of any kind through any of the ventilation slots. Never spill a liquid of any kind on the unit.

This product is equipped with a 3-wire grounding type plug. This is a safety feature and should not be defeated.

Never attach audio power amplifier outputs directly to any of the unit's connectors.

To prevent shock or fire hazard, do not expose the unit to rain or moisture, or operate it where it will be exposed to water.

Do not attempt to operate the unit if it has been dropped, damaged, exposed to liquids, or if it exhibits a distinct change in performance indicating the need for service.

This unit should only be opened by qualified service personnel. Removing covers will expose you to hazardous voltages.

This triangle, which appears on your component, alerts you to the presence of uninsulated, dangerous voltage inside the enclosure... voltage that may be sufficient to constitute a risk of shock.



This triangle, which appears on your component, alerts you to important operating and maintenance instructions in this accompanying literature.

Notice

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designated to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment OFF and ON, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient the receiving antenna
Relocate the computer with respect to the receiver
Move the computer away from the receiver
Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful:

"How to identify and Resolve Radio/TV Interference Problems."

This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class B prescrites dans le Règlement sur le brouillage radioélectrique édicté par le ministère des Communications du Canada.

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Lexicon Part # 070-14826 Rev 0
Printed in the United States of America

Safety Suggestions

Read Instructions Read all safety and operating instructions before operating the unit.

Retain Instructions Keep the safety and operating instructions for future reference.

Heed Warnings Adhere to all warnings on the unit and in the operating instructions.

Follow Instructions Follow operating and use instructions.

Heat Keep the unit away from heat sources such as radiators, heat registers, stoves, etc., including amplifiers which produce heat.

Ventilation Make sure that the location or position of the unit does not interfere with its proper ventilation. For example, the unit should not be situated on a bed, sofa, rug, or similar surface that may block the ventilation openings; or, placed in a cabinet which impedes the flow of air through the ventilation openings.

Wall or Ceiling Mounting Do not mount the unit to a wall or ceiling except as recommended by the manufacturer.

Power Sources Connect the unit only to a power supply of the type described in the operating instructions, or as marked on the unit.

Grounding or Polarization* Take precautions not to defeat the grounding or polarization of the unit's power cord.

*Not applicable in Canada.

Power Cord Protection Route power supply cords so that they are not likely to be walked on or pinched by items placed on or against them, paying particular attention to cords at plugs, convenience receptacles, and the point at which they exit from the unit.

Nonuse Periods Unplug the power cord of the unit from the outlet when the unit is to be left unused for a long period of time.

Water and Moisture Do not use the unit near water — for example, near a sink, in a wet basement, near a swimming pool, near an open window, etc.

Object and liquid entry Do not allow objects to fall or liquids to be spilled into the enclosure through openings.

Cleaning The unit should be cleaned only as recommended by the manufacturer.

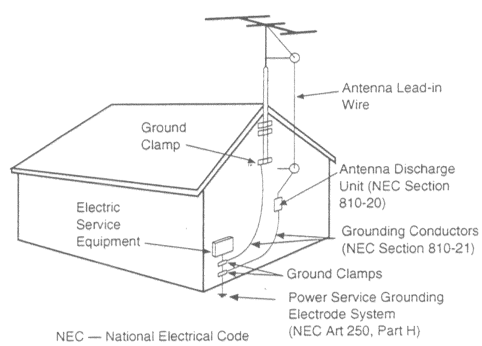
Servicing Do not attempt any service beyond that described in the operating instructions. Refer all other service needs to qualified service personnel.

Damage requiring service The unit should be serviced by qualified service personnel when:

- the power supply cord or the plug has been damaged,
- objects have fallen, or liquid has been spilled into the unit,
- the unit has been exposed to rain,
- the unit does not appear to operate normally or exhibits a marked change in performance,
- the unit has been dropped, or the enclosure damaged.

Outdoor Antenna Grounding If an outside antenna is connected to the receiver, be sure the antenna system is grounded so as to provide some protection against voltage surges and built-up static charges. Section 810 of the National Electrical Code, ANSI/NFPA No. 70-1984, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna-discharge unit, size of grounding conductors, location of antenna-discharge unit, connection to grounding electrodes, and requirements for the grounding electrode. See figure below.

Power Lines An outside antenna should be located away from power lines.



SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service and repair of this instrument. Failure to comply with these precautions, or with specific warnings elsewhere in these instructions violates safety standards of design manufacture and intended use of the instrument. Lexicon assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT

To minimize shock hazard the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor AC power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument.

DANGEROUS PROCEDURE WARNINGS

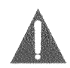
Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing and adjusting.

SAFETY SYMBOLS

General definitions of safety symbols used on equipment or in manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



Indicates dangerous voltage. (Terminals fed from the interior by voltage exceeding 1000 volts must be so marked.)

WARNING — The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION — The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: — The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like which is essential to highlight.



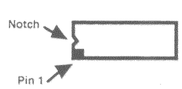
CAUTION

Electrostatic Discharge (ESD) Precautions

The following practices minimize possible damage to ICs resulting from electrostatic discharge or improper insertion.

- Keep parts in original containers until ready for use.
- Avoid having plastic, vinyl or styrofoam in the work area.
- Wear an anti-static wrist-strap.
- Discharge personal static before handling devices.
- Remove and insert boards with care.
- When removing boards, handle only by non-conductive surfaces and never touch open-edge connectors except at a static-free workstation.*
- Minimize handling of ICs.
- Handle each IC by its body.
- Do not slide ICs or boards over any surface.
- Insert ICs with the proper orientation, and watch for bent pins on ICs.
- Use anti-static containers for handling and transport.

*To make a plastic-laminated workbench anti-static, wash with a solution of Lux liquid detergent, and allow to dry without rinsing.



CAUTION

ICs inserted backwards will be destroyed. Incorrect insertion of ICs is also likely to cause damage to the board.

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Chapter 1 Reference Documents, Required Equipment

Reference Documents

960L Owner's Manual - Lexicon P/N 070-14353 or latest revision
Software Release Notice, 960L - Lexicon P/N 070-14354 or latest revision

Required Equipment

Tools

The following is a minimum suggested technician's tool kit required for performing disassembly, assembly and repairs:

- Clean, antistatic, well lit work area.
- (1) #1 Phillips tip screwdriver
- (1) #2 Phillips tip screwdriver
- Small pair chain nose pliers
- Solder: 63/37 - Tin/Lead Alloy composition, low residue, no-clean solder.
- Magnification glasses and lamps
- SMT Soldering / Desoldering bench-top repair station

Test Equipment

The following is a *minimum* suggested equipment list required for performing the proof of performance and diagnostic tests.

- Digital Multi-Meter (DMM)
- Amplifier with speakers or headphones.
- Cables: (dependent on your signal source)
- low distortion analog oscillator
- analog distortion analyzer and level meter with Audio Band-Pass filter
- 100 MHz oscilloscope
- digital distortion analyzer & digital function generator (e.g. Stanford Research Systems Model DS360 or Audio Precision System 1 with DSP Option/System 2).
- Variable AC Power Supply with voltage and current meters,(known as a Variac), adjustable from 0 - 140VAC, and 0-2Amps.BK Precision 1653 or equivalent.
- 100/120 to 220/240 VAC step-up transformer
- LARC2 to 960L Interface Cable, Lexicon P/N 680-03525.
- (2) Male D9 RS422 Wraparound Connectors (see Chapter 5 for spec/drawing)
- (2) audio cables XLR male on one end with appropriate connectors on the opposite end for connection to the low distortion oscillator.
- (2) audio cables XLR female on one end with appropriate connectors on the opposite end for connection to a headphone amplifier.
- Stereo Headphones
- XLR male to XLR female audio cables, maximum length 1 meter.
- XLR male to XLR female audio cables, maximum length 2 meters.
- BNC to BNC Cables, maximum length 5 meters.
- XLR male to XLR female 110 ohm AES digital audio cables, maximum length 1 meter.
- (8) XLR male to XLR female 110 ohm AES digital audio cables, maximum length 2 meters.
- (2) 5 Pin DIN to 5 Pin DIN Cables, maximum length 3 meters, (MIDI Cables), Hosa Technology P/N MID-305 or equivalent.
- Lexicon 960L PCI Extender cards P/N 023-14297
- Lexicon 960L I/O Extender cards P/N 023-14426
- 960L 120V Power Cord, Lexicon P/N 680-09149

- IBM compatible personal computer capable of running Windows 95/98, minimum 200mHz Pentium Processor, 128MB memory, 4GB Hard Disk Drive, SVGA Monitor, Video card w/ 4MB memory, Mouse, 17" monitor, Windows 95 Keyboard, CD-ROM Drive, 3.5" High Density Floppy Disk Drive, and Windows 95/98 Operating System.
- 6' DE-9 Female to DE-9 Female RS-232 Serial Cable.
- DE-9 Male to DE-9 Male RS-232 Null-Modem Adapter
- Female RS-422 Wraparound Plug (see Chapter 5 for spec/drawing)
- PS/2 Keyboard (or IBM 102/104-key keyboard with PS/2 adapter)

- *Optional:*
    - *High Current Continuity Tester, 10A, 100 milliohm. Associated Research 5030DT or equivalent.*
    - *(1) 15" Computer Monitor*
    - *(1) PS/2 Mouse*
    - *LARC2 Option Board (Rev.1), Lexicon P/N 023-14310.*
    - *32MB PCMCIA FLASH Memory Card, PCMCIA 2.1 Compliant, 5 Volt, (LINEAR Flash PC Card, Centennial P/N FL32M-20-11736-J5).*
    - *External Power Supply, 12VDC @ 3A, 5.5 mm O.D., 2.5 mm I.D. barrel connector, with the positive voltage on center contact. PowDec Model WI60-12V or equivalent.*

Chapter 2 General Information

Periodic Maintenance

Under normal conditions the *960L* system requires minimal maintenance. Use a soft, lint-free cloth slightly dampened with warm water and mild detergent to clean the exterior surfaces.

Do not use alcohol, benzene or acetone-based cleaners or any strong commercial cleaners. Avoid using abrasive materials such as steel wool or metal polish. It the unit is exposed to a dusty environment, a vacuum or *low-pressure* blower may be used to remove dust from the unit's exterior.

The 960L's cooling fan, located on the right side of the mainframe (facing the front) has a removable filter. It should be cleaned periodically with water and mild detergent, rinsed thoroughly, dried and reinstalled.

Ordering Parts

When ordering parts, identify each part by type, price and Lexicon Part Number. Replacement parts can be ordered from:

LEXICON, INC.
3 Oak Park
Bedford, MA 01730-1441
Telephone: 781-280-0300; Fax: 781-280-0499; email: csupport@lexicon.com
ATTN: Customer Service

Returning Units to Lexicon for Service

Before returning a unit for warranty or non-warranty service, consult with Lexicon Customer Service to determine the extent of the problem and to obtain Return Authorization. No equipment will be accepted without Return Authorization from Lexicon.

If Lexicon recommends that a *960L* be returned for repair and you choose to return the unit to Lexicon for service, Lexicon assumes no responsibility for the unit in shipment from the customer to the factory, whether the unit is in or out of warranty. All shipments must be well packed (using the original packing materials if possible), properly insured and consigned, prepaid, to a reliable shipping agent.

When returning a unit for service, please include the following information:

- Name
- Company Name
- Street Address
- City, State, Zip Code, Country
- Telephone number (including area code and country code where applicable)
- Serial Number of the unit
- Description of the problem
- Preferred method of return shipment
- Return Authorization #, on both the inside and outside of the package

Please enclose a brief note describing any conversations with Lexicon personnel (indicate the name of the person at Lexicon) and give the name and telephone daytime number of the person directly responsible for maintaining the unit.

Do not include accessories such as manuals, audio cables, footswitches, etc. with the unit, unless specifically requested to do so by Lexicon Customer Service personnel.

Chapter 3 Specifications

960L Mainframe

Analog Input

Connectors	Eight, Female XLR
Impedance	50Kohm, balanced
Level (for 0 dbFS)	+24dBu
Freq Response @48K	20Hz-20KHz, ±1db
Freq Response @96K	20Hz-40KHz, ±1db
A/D Conversion	24 bits 128x oversampled
A/D Dyn Range	**>**110 dB (20-20kHz)
THD	<.002%
CMRR	>50db
Crosstalk @ 1Khz	< -100dB

Analog Output

Connectors	Eight, Male XLR
Impedance	50 Ohm, balanced
Level (at 0 dbFS)	+24dBu
Freq Response @48K	20Hz-20Khz, ±1db
Freq Response @96K	20Hz-40Khz, ±1db
D/A Conversion	24 bits 8x oversampled @ 44.1/48Khz 4x oversampled @ 88.2/96Khz
D/A Dyn Range	**>**110 dB (20-20kHz)
THD	<.002%
Crosstalk @ 1Khz	< -100dB

A/A Performance

Freq Response @48K	20Hz-20Khz, ±1db
Freq Response @96K	20Hz-40Khz, ±1db
Dyn Range	**>**107 dB (20-20kHz)
THD	<.002%

Digital Audio IO

Connectors	Four Male XLR Outputs Four Female XLR Inputs
Format	AES/EBU
Word Size	24 bits

Sample Rates

Internal	44.1/48/88.2/96KHz
Accuracy	within ±10ppm
External	44.1/48/88.2/96KHz
Lock Range	±1%

Group Delays (milliseconds)

	44.1 Khz	48 Khz	88.2 Khz	96 Khz
A/D	1.44	1.33	0.81	0.74
A/A	2.42	2.23	1.80	1.66
D/A	1.54	1.42	1.35	1.25
D/D	0.54	0.50	0.36	0.33

Synchronization

TTL Word Clock Input *
75 Ohm, BNC
self-terminating loopthru

TTL Word Clock Output * Low Z, BNC

(Falling edge marks start of frame)*

Clock Jitter

Intrinsic Exceeds AES3 Amendment 1

Jitter Gain Exceeds AES3 Amendment 1

Control Interfaces

LARC2 Ports 2

MIDI ** In/Out/Thru

*(**supports program change)*

Algorithms

Ambience (48K Stereo & Surround)

Chamber (48K Stereo & Surround)

Plate (48K Stereo & Surround)

Reverse (48K Stereo & Surround)

Random Hall
(48/96K Stereo & 48K Surround)

Ambient Chamber (48K Surround)

Standard Hardware Configuration

DSP/CPU Card Compartment

One System CPU Card
One Reverb DSP Card
Two Spare DSP card slots
One MIDI Card

IO Card Compartment

One Analog Input Card
One Analog Output Card
One AES/EBU Digital IO Card
One IO/Clock Card
One Spare IO Card slot

Storage Media

Hard Disk
3.5” Floppy Disk Drive
CD-ROM Drive

Reverb Card Configurations

48K

Stereo Machines	Four
2in x 5out Machines	Two
5in x 5out Machines	Two
96K	
Stereo Machines	Two
2in x 5out Machines	One
5in x 5out Machines	One

Internal Hard Disk Storage

Factory Programs	240
User Registers	1000

Removable 3.5" Floppy Disk Storage

User Registers	100

Power

Requirements***

100-120 / 220-240 VAC
50-60Hz, 300W max

(some mainframes will have a mains voltage selection switch; if there is no selector switch, it will operate on mains voltages from 100-240 VAC)

Connector	3-pin IEC

Dimensions

Rack Units	4U
Size	19.0" L x 7.0" W x 17.4" H (483mm x 178mm x 442mm)

Weight

35 lbs

Regulatory Approvals

FCC	Class A
CE	EN55103-1, EN55103-2
UL	UL1419
cUL	C22.2
TUV	EN60065

Environment

Operating	10 to 40 °C
Storage	-30 to 70 °C
Humidity	95% max, non-condensing

LARC2 User Interface

Display

Type	Passive Matrix LCD
Resolution	640x240
Colors	256
Backlight	Fluorescent
Contrast	HW controlled (rear panel)
Brightness	SW controlled

LED Meter Bridge

Configuration	8 channels x 3 levels
Levels	
	-60dBFS (Signal)

	-6dBFS
	-0.5dBFS (Overload)

Control Surface

Faders	8
	60mm throw, motorized, touch sensitive
Joystick	Two axis
Dedicated Function Keys	29 (12 backlit)
Soft Buttons	8

Connectors

960L	9-pin D-sub
Aux. PS/2 Keyboard	6-pin Mini-DIN
Ext. Power	concentric, 2.5mm

Operating Distance

With power from 960L	up to100 feet
With Ext. Power	up to1000 feet

Power

Requirements	12 VDC, 3 A (max)

Dimensions

Size	12.7” L x 8.25” W x 5.0” H
	(323mm x 210mm x 127mm)

Weight 4 lbs

Regulatory Approvals

FCC	Class A
CE	EN55103-1, EN55103-2
TUV	EN60065

Environment

Operating	5 to 40 °C
Storage	-30 to 70 °C
Humidity	95% max, non-condensing

Chapter 4 Performance Verification

This section describes the tests and procedures for verification of the operation of the 960L with LARC2 and the integrity of its analog and digital audio signal paths.

Initial Inspection and checkout:

Note: Please refer to the chassis assembly drawing in the Schematics and Drawings section later in this manual.

960L Mainframe:

1. Remove the top and bottom covers of the 960L
2. Inspect the entire unit for obvious signs of physical damage.
3. Unscrew the front panel screws and fold down the front panel.
4. Verify that the main processor board, midi card, and reverb cards are seated properly and are held down with screws. Also verify that all cable connections to the midi card, main processor board, and backplanes are in place.
5. At the back of the unit, in the power supply section, verify that all connections are firmly seated to the backplane. Verify all ribbon cables are firmly seated to the I/O backplane and that Pin 1 of all ribbon cables (identified by a red stripe) are at the top of the connectors.
6. Carefully turn the unit over.
7. Verify that all of the drives are properly secured in place. Verify all ribbon cables and power cables to these devices are firmly seated.
8. Verify all ribbon cables to both the NLX and I/O backplanes are firmly seated.
9. On the back panel of the 960L make sure all cards are tightly screwed in place. Inspect all connectors for wear or breaks that might cause intermittent operation.

LARC2 controller:

1. Inspect the entire unit for obvious signs of physical damage such as cracked or broken plastic housings.
2. Verify display is not cracked or shattered.
3. Verify all sliders move up and down smoothly and do not bind.
4. Verify the joystick also has a smooth, fluid movement.
5. Depress all the buttons to insure non-stick operation.

Cables:

Inspect both the 960L power cable and LARC cable for physical damage or excessive wear.

Power Supplies:

Note: It is important that the power supply be tested while fully connected in the 960L mainframe to insure proper voltage readings.

System Current Draw Tests:

1. For 100/120V operation, verify that the voltage selection switch* on the back of the 960L is set to the 115 Volt setting.
2. Set the voltage level on the Variable AC power supply down to 0 volts then turn it ON.
3. Plug the 960L into the variable AC power supply and switch the main power switch on the rear panel to the ON position.
4. Slowly bring the variable AC power supply voltage up to 120 Volts. The current draw will vary from between approximately 0.5A and 1.5A.
5. At 120V verify that the current draw is approximately 0.75 A and that the Green Power On LED above the Front Panel power switch is on.
6. Power off.

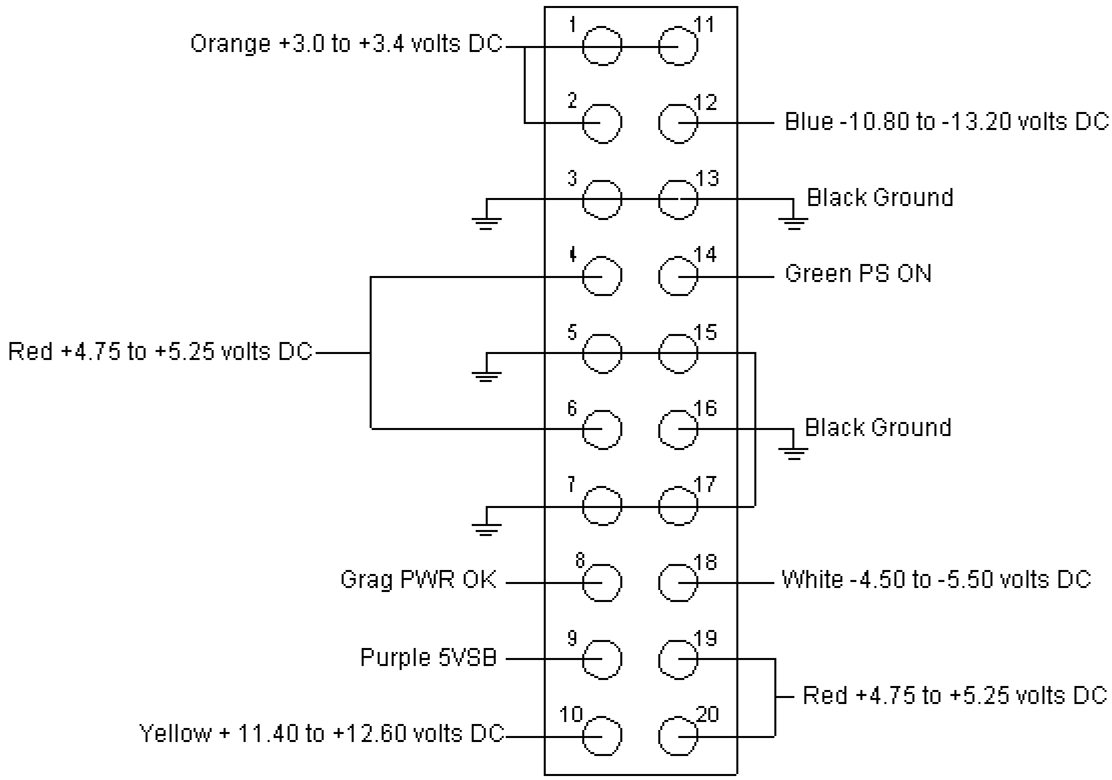
7. For 220/240V operation, verify that the voltage selection switch* on the back of the 960L is set to the 230 Volt setting.
8. Follow steps 2 through 6 above. Note - the current draw should be approximately one-half of that listed in the steps above dependant upon the accuracy of the current meter. It should not be higher.

*Note: Different manufacturer's power supplies have been specified for the 960L. There are some slight mechanical differences in some of these power supplies. Some units will have a power supply with a voltage setting switch as noted above. Some units will have a power supply that does not have a voltage selection switch. The AC voltage input will be automatically sensed by the supply. Be sure to inspect the unit in case of the need to "switch" for the appropriate AC input voltage.

Main Power Supply Connector J26 Voltage Level Tests:

1. Remove the top and bottom covers of the 960L.
2. Remove all DSP cards and the Midi card from the card cage in the front section of the 960L and place them in static shielding bags.
3. With the front of the 960L facing you, locate the solder side of connector J26 on the Left side of the NLX backplane.
4. Clip the ground lead of the DMM meter to the chassis for ground reference.
5. Take the Plus lead and using the table below verify the voltage levels indicated on J26.

Pin #	Wire Color	Voltage Range
1	Orange	+ 3 volts DC +.4/-0
4	Red	+ 5 volts DC ±.25
10	Yellow	+ 12. volts DC ±.6
12	Blue	-12 volts DC ±1.2
13	Black	Ground
18	White	- 5 volts DC ±.5



NOTE: The following voltage tests are to insure that the connectors are plugged into the NLX backplane and that power is being properly distributed to the other devices. This may also help in determining whether or not the devices themselves are defective.

To gain easier access to the test points called out in the following tests, you will want to turn over the mainframe of the 960L so the bottom faces up or rest it on its side.

All power connections to the backplane, Hard Drive, CD ROM Drive and 3.5" Floppy Drive have the same colored wiring code.

Color	Voltage Range
Yellow	+ 12. volts DC ±.6
Black	Ground
Red	+ 5 volts DC ±.25

NLX Backplane Connector J9 Voltage Level Test:

1. Locate the power connector J9 on the rear backplane.
2. Measure the voltages on the connector with your DMM leads.
3. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Yellow wire connector and verify the voltage is +12 VDC (± .6 VDC).
4. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Red wire connector and verify the voltage is + 5 VDC (± .25 VDC).

3.5" Floppy Drive Connector:

1. Locate the power connector on the back of 3.5” Floppy Drive.
2. With your DMM leads measure the voltages on the connector.

3. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Yellow wire connector and verify the is +12 VDC (± .6 VDC).
4. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Red wire connector and verify the voltage is +5 VDC (± .25 VDC).

CD-ROM Drive Connector:

1. Locate the power connector on the back of CD-ROM drive.
2. With your DMM leads measure the voltages on the connector.
3. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Yellow wire connector and verify the voltage is +12 VDC (± .6 VDC).
4. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Red wire connector and verify the voltage is +5 VDC (± .25 VDC).

Hard Drive Connector:

1. Locate the power connector on the back of Hard Drive.
2. With your DMM leads measure the voltages on the connector.
3. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Yellow wire connector and verify the voltage is +12 VDC (± .6 VDC).
4. Place the DMM ground lead on the Black wire connector and the DMM plus lead on the Red wire connector and verify the voltage is +5 VDC (± .25 VDC).

For the following voltage tests, an I/O extender card (part # 023-14426) will be needed to bring the cards out of the mainframe in order to gain access to the test points called out in the following tests.

Analog Output Card Voltage Test:

The supplies being tested on this card will be the +/-12 VSUP, and the +5VD provided by the main supply via the backplane and voltages +5VD, 6.6V, +/-18V, 24V, and 36V created on the card.

1. Before powering on the 960L for this test, remove the Analog Output card from the rear of the chassis.
2. Insert the I/O extender card and install the Analog Output card into the extender card.
3. Power on the 960L.
4. For your ground reference locate test point marked GND to the Left of U3.
5. At the back right hand corner of the card locate the –12V-test point just below FB2. Verify the voltage is -12VDC ±1.2VDC.
6. Next locate in the test point marked +12V just below FB3. Verify the voltage is +12VDC ±.6VDC.
7. Locate the +5VD voltage test point left side of the card just above U6. Verify the voltage is +5VDC ±.25VDC.
8. Locate the +5 VA voltage test point just below U3 between D8 and D9. Verify the voltage is +5VDC ±.25VDC.
9. Locate the + VB voltage test point on the right side of the card just to the left of C15. Verify the voltage is between + 6.27 and + 6.93 VDC.
10. Locate the +/- VCC voltage test points on the right side of the card. +VCC is just to the right of C206 and –VCC is just to the right of that under FB54. Verify the voltage to be +17.50VCC and -17.50VCC +/- 1.0 volt each.

Analog Input Card Voltage Test:

The supplies being tested on this card will be the +/- 12 VSUP provided by the main supply via the backplane and the +5VD, and +5VA created on the card.

1. Before powering on the 960L for this test, remove the Analog Input card from the rear of the chassis.
2. Insert the I/O extender card and install the Analog Input card into the extender card.
3. Power on the 960L.
4. For your ground reference, locate test point marked GNDA just above D7.

5. At the back right hand corner of the card locate the FB1. Measure the +12 volts here and verify the voltage is +12VDC ± .6VDC.
6. Next locate FB2. Measure the -12 volts here and verify the voltage is -12VDC ± 1.2VDC.
7. Using the same ground reference measure pin 3 of U3 (+ 5 VA). Verify the voltage is +5VDC ± .25VDC.
8. Locate the + 5 VD test point on the left side of the card just to the left of U1. Using the ground reference marked GNDD2 just to the right of the + 5 VD verify the voltage is +5VDC ± .25VDC.

AES Input /Output Card Voltage Test:

The supply being tested on this card will be the +5VD provided by the main supply via the backplane.

1. Before powering on the 960L remove the AES Input/Output card from the rear of the chassis.
2. Insert the I/O extender card and install the AES Input/Output card into the extender card.
3. Power on the 960L.
4. Locate the ground reference test point marked GND1 just above U3.
5. Locate test point marked + 5 V to the right of the GND1 test point.
6. With the DMM verify the voltage is +5VDC ± .25VDC.

Input/Output Clock Generator Card Voltage Test:

The supplies being tested on this card will be the +/-12 VSUP and the +5VD provided by the main supply via the backplane.

1. Before powering on the 960L remove the Input/Output Clock card from the rear of the chassis.
2. Insert the I/O extender card and install the Input/Output Clock card into the extender card.
3. Power on the 960L.
4. For a ground reference locate test point marked GND2 on the right side of the card.
5. Locate the ferrite bead FB3 at the back of the card just to the right of the connector and measure the +12 volts. Verify the voltage is +12VDC ± .6VDC.
6. FB4 is next to FB3. Measure the -12 volts here. Verify the voltage -12VDC ± 1.2VDC.
7. Locate the ground reference test point marked GND1 on the left side of the card just to the left of U1.
8. Locate test point marked + 5 V just below U1.
9. With the DMM verify the voltage is +5VDC ± .25VDC.

Audio/Functional Tests Setup*:

1. Power on the 960L with the main power switch and wait for the Power on diagnostics cycle to finish.
2. On the Larc2, press the Control Button. The Control Mode screen will appear at this time.
3. Press the #1 button to set the clock source to Internal. Note: for any "Digital In" tests, you will need to return to this screen and select Source #3, **AES/EBU**.
4. Press the Right arrow button to jump to the Rate page.
5. Press the #2 button to select a 48kHz sample rate.
6. Press the Soft button labeled CONFIG under the display.
7. Press the #4 button. This will highlight the 1-8in/8out setup for Diagnostics.
8. Press the Edit button, the screen will then display the Edit Mode page
9. Press the Soft button labeled Algorithm, the display will then read Algorithms Options Enabled.
10. Press the Soft button labeled Select, a small box will open with 1-OctalThru stated.
11. Press the #1 button, then the Enter button this will load the Diagnostic 1-8in/8out setup.
12. Press Control and then the ►key to highlight Inputs.
13. Press the + key to toggle the state to **AN** (Analog). Note: for any "Digital In" tests, you will need to return to this screen and toggle the state to **AES** (Digital).
14. Set the distortion analyzer to measure VRMS.

***Note: The following tests should also be performed at the 44.1kHz and 96kHz sample rates. Prior to performing the following tests at each sample rate, you must perform the previous set-up procedure substituting the indicated sample rate in step 5.**

I/O Gain Tests

Analog In to Analog Out Audio Gain Test:

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 1kHz sinewave @ 9.75 VRMS.
4. Verify the output level to be 10 VRMS ±1.5V.
5. Repeat the test on the remaining Input /Outputs 2-8.

Analog In To Digital Out Audio Gain Test:

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1-2 AES Output and the digital distortion analyzer.
3. Apply a 1kHz sinewave @ 10.94 VRMS.
4. Verify the output level to be -1 dBFS ± 1dBFS.
5. Move the audio input cable to the # 2 Input and repeat the test.
6. Repeat the test on the remaining Input /Outputs pairs 3-4, 5-6, and 7-8.

Digital Input to Analog Output Gain Test:

Note: Change the Clock Source and Inputs to AES - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the digital function generator and the 960L # 1-2 AES Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 1kHz sinewave @ -1 dBFS.
4. Verify the output level to be 11.5 VRMS ±1.5V.
5. Move the audio output cable to the # 2 Output and repeat the test.
6. Repeat the test on the remaining Input /Outputs pairs 3-4, 5-6, and 7-8.

Frequency Response:

Analog In to Analog Out Frequency Response Test:

Note: Change the Clock Source to Internal and Inputs to Analog - see Audio/Functional Tests Setup.

1. Disable all filters on the distortion analyzer.
2. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
3. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
4. Apply a 1kHz sinewave @ 2.45 VRMS.
5. Set the Analyzer for a 0dB reference (@1khz)
6. Sweep the oscillator from 20Hz to 20kHz and verify the level is +/- 1dBr throughout the sweep.
7. Repeat the test on the remaining Input /Outputs 2-8.

Analog In To Digital Out Frequency Response Test:

1. Disable all filters on the digital distortion analyzer.
2. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
3. Connect a balanced XLR audio cable between the 960L # 1-2 AES Output and the digital distortion analyzer.
4. Apply a 1kHz sinewave @ 6.90 VRMS.
5. Set the Analyzer for a 0dB reference (@1khz)
6. Sweep the oscillator from 20Hz to 20kHz and verify the level is +/- 1dBr throughout the sweep.

7. Move the Audio Input cable to Audio Input #2 and repeat the test.
8. Repeat the test on the remaining Input /Outputs pairs 3-4,5-6, and 7-8.

Digital In To Analog Out Frequency Response Test:

Note: Change the Clock Source and Inputs to AES - see Audio/Functional Tests Setup.

1. Disable all Filters on the distortion analyzer
2. Connect a balanced XLR audio cable between the digital function generator and the 960L # 1-2 AES Input.
3. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
4. Apply a 1kHz sinewave @ -1 dBFS.
5. Set the Analyzer for a 0dB reference (@1khz)
6. Sweep the oscillator from 20Hz to 20kHz and verify the level is +/- 1dBr throughout the sweep.
7. Move the audio output cable to the # 2 Output and repeat the test.
8. Repeat the test for the remaining Input /Outputs pairs 3-4,5-6, and 7-8.

THD+N Measurement:

Analog In to Analog Out THD+N Test:

Note: Change the Clock Source to Internal and Inputs to Analog - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 997Hz sinewave @ 9.75 VRMS.
4. Set the distortion analyzer to measure THD+N.
5. Enable the Audio Band Pass filter on the distortion analyzer.
6. Verify the output THD+N on the Analyzer is < 0.002%.
7. Repeat the rest for the remaining Input /Outputs 2-8.

Analog In to Digital Out THD+N Test:

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1-2 AES Output and the digital distortion analyzer.
3. Apply a 997Hz sinewave @ 10.94 VRMS.
4. Set the distortion analyzer to measure THD+N.
5. Enable the Audio Band Pass filter on the distortion analyzer.
6. Verify the output THD+N on the Analyzer is < -94 dBFS.
7. Move the audio input cable to the # 2 Input and repeat the test.
8. Repeat the test for the remaining Input /Outputs pairs 3-4,5-6, and 7-8.

Digital In to Analog Out THD+N Test:

Note: Change the Clock Source and Inputs to AES - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the digital function generator and the 960L # 1-2 AES Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 997Hz sinewave @ -1 dBFS.
4. Set the distortion analyzer to measure THD+N.
5. Enable the Audio Band Pass filter on the distortion analyzer.
6. Verify the output THD+N on the Analyzer is < -94 dBFS.
7. Move the audio output cable to the # 2 Output and repeat the test.
8. Repeat the test for the remaining Input /Outputs pairs 3-4,5-6, and 7-8.

Crosstalk Tests:

Analog In to Digital Out Crosstalk Test:

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1-2 AES Output and the digital distortion analyzer.
3. Apply a 997Hz sinewave @ 10.94 VRMS.
4. Enable the Audio Band Pass filter on the distortion analyzer.
5. Verify the level on AES Output #2 to be < -100 dB throughout the sweep.
6. Move the Input cable to the # 2 Input and repeat the test for AES Output #1.
7. Repeat the test for the remaining Input /Outputs pairs 3-4, 5-6, and 7-8.

Digital In to Analog Out Crosstalk Test:

Note: Change the Clock Source and Inputs to AES - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the digital function generator and the 960L # 1-2 AES Input.
2. Connect a balanced XLR audio cable between the 960L # 2 Audio Output and the distortion analyzer.
3. Apply a 997Hz sinewave @ -1 dBFS.
4. Enable the Audio Band Pass filter on the distortion analyzer.
5. Verify the level on Output #2 to be < -100 dB throughout the sweep.
6. Move the audio output cable to the # 1 Output and repeat the test.
7. Repeat the test for the remaining Input /Outputs pairs 3-4,5-6, and 7-8.

Dynamic Range Tests:

Analog In to Analog Out Dynamic Range Test:

Note: Change the Clock Source to Internal and Inputs to Analog - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 997Hz sinewave @ 24dBu.
4. Set the distortion analyzer for a 0dB reference.
5. Enable the Audio Band Pass filters on the distortion analyzer.
6. Lower the input by 60dB to -36dBu.
7. Verify the THD+N at the # 1 output to be <-110 dBr.
8. Repeat the test for the remaining Input/Outputs 2-8.

Analog In to Digital Out Dynamic Range Test:

1. Connect a balanced XLR audio cable between the low distortion oscillator and the 960L # 1 Audio Input.
2. Connect a balanced XLR audio cable between the 960L # 1-2 AES Output and the digital distortion analyzer.
3. Apply a 997Hz sinewave @ 24dBu.
4. Set the distortion analyzer for a 0dB reference.
5. Lower the input by 60 dB to -36dBu.
6. Verify the THD+N level at the # 1-2 AES Output to be <-110 dBFS.
7. Move the audio input cable to the # 2 Input and repeat the test.
8. Repeat the test for the remaining Input /Outputs pairs 3-4, 5-6, and 7-8.

Digital In To Analog Out Dynamic Range Test:

Note: Change the Clock Source and Inputs to AES - see Audio/Functional Tests Setup.

1. Connect a balanced XLR audio cable between the digital function generator and the 960L # 1-2 AES Input.
2. Connect a balanced XLR audio cable between the 960L # 1 Audio Output and the distortion analyzer.
3. Apply a 997Hz sinewave @ -1 dBFS.
4. Set the distortion analyzer for a 0dB reference.
5. Enable the Audio Band Pass filter on the distortion analyzer.
6. Lower the input by 60dB to -61dBFS.
7. Verify the THD+N at the # 1 output to be < -110 dB.
8. Move the audio output cable to the # 2 Output and repeat the test.
9. Repeat the test for the remaining Input /Outputs pairs 3-4, 5-6, and 7-8.

Functional Tests:

Midi Tests:

Setup

1. This test will require 1 Midi cable. The cable is connected to the Midi In and Out connector on the back of the 960L creating a loop that the internal diagnostics requires to perform the test.
2. The 960L must first be placed into Diagnostic mode. This is done by powering on the 960L's main power switch on the rear panel, then immediately pressing and holding down the Program and Machine buttons on the LARC2 for 2 seconds. When the LARC2 displays "Requesting Menu Mode …", the buttons can be released. The display will take about two minutes, then it should state the following:
   960L Boot Menu - Version ### Speed ### BIOS date ##/##/##
   [Note: ### are placeholders for actual values which may vary]
   1) Run 960L
   2) Update 960L Software
   3) Update LARC2 Boot ROM
   4) Update LARC2
   5) 960L Diagnostics

   Can't lock CD Drive: Access is denied

3. Press the # 5 button to enter the Diagnostics.
4. The display will scroll through some information then settle. At the bottom of the display it will read, Press 0 for a list of tests.
5. Press the # 9 on the LARC2 then the Enter button.
6. If the Midi circuitry is good the display will read
   MIDI Test : Passed
   All test PASSED

   If it fails then the display will read
   MIDI Test : Failed : No data received
   One or more tests failed
7. To exit Diagnostics, power off, then power on the unit.

Listening Test:

Setup:

1. Connect the two audio XLR male cables from the low distortion oscillator to Analog Inputs marked 1 and 2 on the back of the 960L.
2. Connect the two audio XLR female cables from the Headphones Amplifier to the Analog Outputs marked 1 and 2 on the back of the 906L.
3. Set the oscillator to 220Hz @ 2.5VRMS.

4. Turn the volume control on the Headphone Amplifier completely counter-clockwise, and plug in the stereo headphones.
5. Power on the 960L.
6. Configure the 960L as follows. Control Mode to Stereo, Program load Bank 12 Halls, then load program #1 Large Halls.

Verify Clean Audio:

1. Put on Headphones
2. Press the Edit button on the LARC2 make sure the Mix/Wet slider is set to Wet
3. Slowly increase the volume on the Headphone Amplifier unit it's at a comfortable listening level.
4. Slowly sweep the oscillator across the audio frequency band and verify that no pops, clicks, static, hash, and breakup in the audio.
5. Move the input and output cables to the next machine pair of the 960L (3,4) (5,6) and (7,8).
6. Repeat the test for each paired output.

Shock Test:

1. While still listening with the headphones. Lift each corner to the 960L a few inches off the workbench and drop.
2. Verify there is no audio break up.
3. Inspect all components after to be sure nothing was loosened by this test.

Lexicon Audio Precision ATE Summary

Test Name	SOURCE Analog or Digital Generator Left	Right	Freq (hz)	Z-out	Bal/ Unbal	Gnd/ Float	ANALYZER Analog or Digital Analyzer Level	Measure	Typ Read	Upper Limit	Lower Limit	Filter	Imp.	Band.	960L Setup Configuration	Algorithm	Clock Source	Sample Rate	Audio Source
Mute Test	**Analog Generator**						**Analog Analyzer**												
960lmute	n/a	n/a	n/a	n/a	n/a	n/a	dBu	Level	-999	-100	-2000	n/a	100k	<10 - >500k	n/a	n/a	n/a	n/a	n/a
A-D 48 kHz Internal Sam	**Analog Generator**						**Digital Analyzer**												
a-d 48k gain	23dBu	23dBu	997	40	Bal	Gnd	dBFS	Level	-1	0	-2	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	48000	Analog
a-d 48k freq resp	19dBu	19dBu	20-20k	40	Bal	Gnd	dBr	Level	0	1	-1	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	48000	Analog
a-d 48k thd+n	23dBu	23dBu	20-20k	40	Bal	Gnd	dBFS	THD+N	-110	-94	-120	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	48000	Analog
a-d 48k dyn-rng	-36dBu	-36dBu	20-20k	40	Bal	Gnd	dBFS	THD+N	-113	-110	-130	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	48000	Analog
a-d 48k cmrr	23dBu	23dBu	997	40	CMTST	Gnd	dBu	Level	-70	-50	-100	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	48000	Analog
a-d 48k xtalk	23dBu	23dBu	997	40	Bal	Gnd	dBu	Level	-140	-100	-150	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	48000	Analog
A-D 44.1 kHz Internal Sample Rate Tests																			
a-d 44k gain	23dBu	23dBu	997	40	Bal	Gnd	dBFS	Level	-1	-0.5	-1.5	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	44100	Analog
a-d 44k thd+n	23dBU	23dBu	20-20k	40	Bal	Gnd	dBFS	Level	-110	-94	-120	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	44100	Analog
a-d 44k dyn-rng	-36dBu	-36dBu	20-20k	40	Bal	Gnd	dBFS	THD+N	-113	-110	-130	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	44100	Analog
A-D 96 kHz Internal Sample Rate Tests																			
a-d 96k gain	23dBu	23dBu	997	40	Bal	Gnd	dBFS	Level	-1	-0.5	-1.5	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	96000	Analog
a-d 96k freq resp	19dBu	19dBu	20-40k	40	Bal	Gnd	dBr	Level	0	1	-1	n/a	n/a	<10 - Fs/2	8 In 8 Out	OctalThru	Internal	96000	Analog
a-d 96k thd+n	23dBu	23dBu	20-20k	40	Bal	Gnd	dBFS	THD+N	-110	-94	-120	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	96000	Analog
a-d 96k dyn-rng	-36dBu	-36dBu	20-20k	40	Bal	Gnd	dBFS	THD+N	-113	-110	-130	n/a	n/a	<10Hz->20kHz LP	8 In 8 Out	OctalThru	Internal	96000	Analog
D-A 48 kHz AES Sample	**Digital Generator**						**Analog Analyzer**												
d-a 48k gain	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBu	Level	23.5	24.5	22.5	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	48000	AES
d-a 48k freq resp	-1dBFS	-1dBFS	20-20k	n/a	n/a	n/a	dBr	Level	0	1	-1	n/a	100k	<10 - >500k	8 In 8 Out	OctalThru	AES	48000	AES
d-a 48k thd+n	-1dBFS	-1dBFS	20-20k	n/a	n/a	n/a	%	THD+N	0.0004	0.002	0.0001	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	48000	AES
d-a 48k dyn-rng	-60dBFS	-60dBFS	20-20k	n/a	n/a	n/a	dBr	THD+N	-113	-110	-120	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	48000	AES
d-a 48k xtalk	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dB	Level	-140	-100	-150	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	48000	AES
D-A 44.1 kHz AES Sample Rate Tests																			
d-a 44k gain	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBu	Level	23.5	24.5	22.5	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	44100	AES
d-a 44k thd+n	-1dBFS	-1dBFS	20-20k	n/a	n/a	n/a	%	THD+N	0.0004	0.002	0.0001	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	44100	AES
d-a 44k dyn-rng	-60dBFS	-60dBFS	20-20k	n/a	n/a	n/a	dBr	THD+N	-113	-110	-120	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	44100	AES
D-A 96k AES Sample Rate Tests																			
d-a 96k gain	-1dBFS	-1dBFS	997	n/a	n/a	n/a	dBu	Level	23.5	24.5	22.5	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	96000	AES
d-a 96k freq resp	-1dBFS	-1dBFS	20-40k	n/a	n/a	n/a	dBr	Level	0	1	-1	n/a	100k	<10 - >500k	8 In 8 Out	OctalThru	AES	96000	AES
d-a 96k thd+n	-1dBFS	-1dBFS	20-20k	n/a	n/a	n/a	%	THD+N	0.0006	0.002	0.0001	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	96000	AES
d-a 96k dyn-rng	-60dBFS	-60dBFS	20-20k	n/a	n/a	n/a	dBr	THD+N	-113	-110	-120	n/a	100k	<10 - 22k	8 In 8 Out	OctalThru	AES	96000	AES
BNC Thru Tests	**Digital Input/Output**						**Analog Analyzer**												
word clk thru gain	2.500 Vpp	48000	n/a	n/a	n/a	n/a	Vpp	Level	2.500	2.60	2.3	n/a	n/a	n/a	8 In 8 Out	OctalThru	BNC	n/a	n/a
word clk thru freq	Output	Sample	Rate	Sweep	100k-40k	n/a	Hz	Freq	100k - 40k	+50	-50	n/a	n/a	n/a	8 In 8 Out	OctalThru	BNC	100k - 40k	n/a
D-A BNC Word Clock Ou	**Digital Generator**						**Analog Analyzer**												
d-a 48k word clk out thd+n	-1dBFS	-1dBFS	997	n/a	n/a	n/a	%	THD+N	0.0006	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	Internal	48000	AES
d-a 44k word clk out thd+n	-1dBFS	-1dBFS	997	n/a	n/a	n/a	%	THD+N	0.0006	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	Internal	44100	AES
D-A BNC Word Clock In Sample Rate Tests																			
d-a 48k word clk in thd+n	-1dBFS	-1dBFS	997	Sweep	48.495k to	47.505k	%	THD+N	0.0004	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	BNC	48,975-47,0250	AES
d-a 44k word clk in thd+n	-1dBFS	-1dBFS	997	Sweep	44554k to	43.646k	%	THD+N	0.0004	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	BNC	45,000-43,200	AES
D-A BNC 96k Word Clock In/Out Sample Rate Tests																			
d-a 96k word clk in thd+n	-1dBFS	-1dBFS	997	Sweep	96.989k to	95.011k	%	THD+N	0.0006	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	BNC	97,950-94,050	AES
d-a 96k word clk out thd+n	-1dBFS	-1dBFS	997	n/a	n/a	n/a	%	THD+N	0.0006	0.002	0.0001	Off	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	Internal	96000	AES
A-A Tests	**Analog Generator**						**Analog Analyzer**												
a-a gain	22dBu	22dBu	997	40	Bal	Gnd	dBu	Level	22.5	23.5	21.5	n/a	100k	<10Hz->500kHz	8 In 8 Out	OctalThru	Internal	48000	Analog
a-a freq resp	10dBu	10dBu	20-20k	40	Bal	Gnd	dBr	Level	0	1	-1	n/a	100k	<10Hz->500kHz	8 In 8 Out	OctalThru	Internal	48000	Analog
a-a thd+n	22dBu	22dBu	20-20k	40	Bal	Gnd	%	THD+N	0.0006	0.002	0.0001	n/a	100k	<10Hz-22kHz	8 In 8 Out	OctalThru	Internal	48000	Analog
Listen Test	**Analog Generator**						**Analog Analyzer**												
960 Listen	15dBu	15dBu	500	40	Bal	Gnd	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Stereo Thru	Random Hall	Internal	48000	Analog

Chapter 5 Service Notes

Motherboard - lithium battery

The motherboard has a lithium battery. This is not user replaceable. Only a qualified service technician should replace it. Lithium batteries may be considered a hazardous substance should be disposed of in accordance with any local, national or international laws or guidelines.

Power Supplies

Various manufacturer's power supplies have been specified for the 960L. There are some slight mechanical differences in some of these power supplies. Some units will have a power supply with a voltage setting switch as noted above. Some units will have a power supply that does not have a voltage selection switch and the AC voltage input will be automatically sensed by the supply. Always be sure to inspect the rear panel of the 960L for indication of proper AC voltage setup and in case of the need to "switch" for the appropriate AC input voltage.

Symptoms of possible power supply failures

1. The fan mounted on the processor of the Main PC card and the fan mounted on the right side of the chassis are spinning in slow motion or not spinning at all.
2. The Larc2 is indicating not seeing the 960L mainframe.

If supply problems are suspected, please test for proper voltage reading with a DMM meter as described in the Troubleshooting section of this service manual.

Larc2 Meter Display LED Handling

Due to the special storage and handling procedures required for these dry packed moisture sensitive devices and the sensitivity to temperature, Lexicon recommends that the Meter Board Assembly be replaced in its entirety when service of the LEDs is required. Spare modules can be obtained from the factory, Lexicon P/N 021-14511.

Removal and Replacement of Larc2 Piezo Transducer

For units with the transducer soldered (Rev 5 PCB and up):

Removal

1. Wick the solder from the transducer and the PCB solder pads.
2. Re-flow the remaining solder while gently lifting the transducer edge with an X-acto blade.

Replacement

1. Prep the PCB solder pads as needed
2. Assemble the transducer as outlined in the assembly notes on DWG # 080-14234, ASSY DWG, MECH, MAIN BD, LARC 2
3. Solder the transducer to the six pads provided.

NOTE: Solder the pads alternately across from each other to minimize overheating of the transducer

For units with the transducer epoxied (Rev 4 PCB and below):

Removal

1. Gently insert the blade between the PCB and transducer to pry it loose from the 5-minute epoxy.

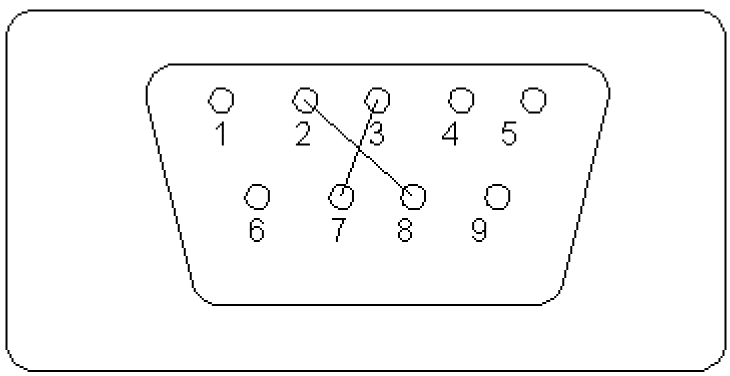
Replacement

1. Assemble the transducer as outlined in the assembly notes on DWG # 080-14234, ASSY DWG, MECH, MAIN BD, LARC 2

Female RS-422 Wraparound Plug:

Female RS-422 Wraparound Plug

Solder Side View



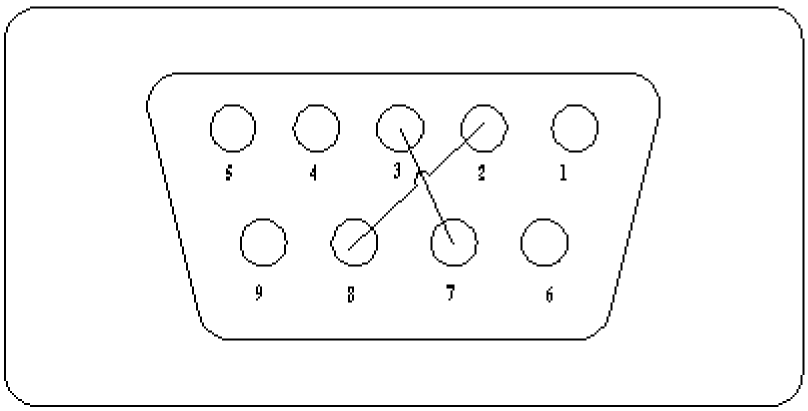
Female DB-9
AmphenolP/N
17S-DE-9S

Instructions: Using 24AWG buss wire or equivalent, solder pin 2 to 8 and pin 3 to 7.

Male RS-422 Wraparound Plug

MALE RS-422 Wraparound Connector

Solder Side View



Male D-Sub 9 Pin
Amphenol P/N
17S-DE-09S

Instructions: Using 24 - 28 AWG buss wire or equivalent, solder pins 2 to 8 and 3 to 7.

Chapter 6 Troubleshooting

Check the Lexicon web site and Customer Support Knowledgebase for the latest software and information:
http://www.lexicon.com
http://www.lexicon.com/kbase/kbase.asp

Diagnostics

Overview

The purpose of this document is to describe the diagnostic tests in the 960L. The diagnostics in the 960L are utilized to verify performance and functionality. The 960L and LARC2 are a high end, digital audio effects system. The 960L and LARC2 system is a multi-channel digital audio effects processor that can also be configured as a single channel processor. The LARC2 provides full control of 960L through a 50-foot, 9-pin cable. The 960L and LARC2 system is composed of the following printed circuit assemblies manufactured by Lexicon:

1. NLX backplane
2. I/O backplane
3. I/O Clock
4. Analog In
5. Analog Out
6. Reverb
7. AES
8. LARC2 Main
9. LARC2 Meter.

In addition there are 6 OEM devices:

1. NLX PC processor card (motherboard) with Celeron CPU Processor
2. NLX/ATX power supply
3. 3.5” floppy drive
4. CD-ROM
5. MIDI Card
6. Hard Disk Drive

960L Diagnostics:

The 960L has 3 sets of diagnostics, power on, functional, and troubleshooting. The power on diagnostics are executed every time the 960L is powered on. The power on diagnostics verify basic reverb card functionality, checks which cards are present in the I/O cage and communicates with the LARC2.

The functional diagnostics are used to verify the performance of the digital circuitry of the 960L. The functional diagnostics test the following:

1. MIDI port
2. Serial 2 Port
3. Reverb Card, which includes
    a. 56301 to Dual Port Ram
    b. Z80 to Dual Port Ram
    c. Z80 to DRAM
    d. Z80 to SRAM
    e. Lexichip3 WCS, (Writeable Control Storage)
    f. Lexichip3 ADF, (Audio Data File)
    g. TMIX
    h. Serial Audio, (all the Octal Audio Data lines)

4. I/O Cage Cards

The functional diagnostics test the hardware on the 960L that do not process audio, as well as the audio processing circuitry. The non-audio processing sections include the MIDI, clock ports, and serial communication on 960L. The audio processing is verified with functional diagnostics and a dry audio-processing algorithm available in the normal operating mode called 8 In 8 Out. Diagnostic testing is performed on the 960L prior to burn-in.

The troubleshooting diagnostics are those tests that are available to assist a technician, either in-house or in another part of the world, to debug a 960L to the component level.

960L Diagnostic User Interface:

The primary user interface for the 960L diagnostics is the LARC2. The secondary user interface for the diagnostics are the LED's on the Reverb card, which indicate Reverb functionality. Lastly a computer monitor can be connected to the NLX motherboard video port in order to change BIOS settings.

Pressing together and holding for 2 seconds the PROGRAM and MACHINE buttons on the LARC2 immediately after powering on the 960L enters the diagnostics. When the LARC 2 displays Requesting Menu Mode from 960L . . ., the buttons can be released. In approximately 1 minute 30 seconds the LARC2 will display the following boot menu:

960L Boot Menu - Version: X.XX Speed: XXX MHz BIOS: 11/22/99

1) Run 960L
2) Update 960L Software
3) Update LARC2 Boot ROM
4) Update LARC2 Software
5) 960L Diagnostics

Can't lock CD Drive: Access is denied

The Version refers to the latest version of the boot menu that is running. The current version is 1.00R, however this may change without requiring this document to be updated. The speed refers clock speed of the Celeron processor. This value is 1-3 MHz below the actual value. So a value of 398 MHz would actually be a 400 MHz Celeron. The date after the BIOS refers to the date of the Intel SU810 BIOS. Currently version 5 of the BIOS dated 11/22/99 is the version required running on the 960L.

Pressing the 5 button on the LARC2 enters diagnostics. The display will appear similar to the sample below on the LARC2 upon entering the diagnostics:

Lexicon 960L Diagnostics
Version X.XX MM DD YYYY HH:MM:SS
****
*Chameleon Configuration *
****
VxD Version = 6A
Num Cards = 1
<u>Card 0 Configuration</u>
Config Valid . . . YES
Subvendor ID . . .4863
56301 IDR 0x2301
DB Type . . . . . . .Lexichip III

DB Version 2

IO Card Info:
Card 0: Clock Version *X*
Card 1: unknown
Card 2: AES Version *X*
Card 3: Analog In Version *X*
Card 4: Analog Out Version *X*

Press 0 for a list of tests.

>

The text below Card 0 Configuration, verifies that a reverb card is present and can be identified by the diagnostics. After that the cards in the I/O cage are identified. At this point if the reverb card cannot be identified, look at the 4 leftmost LEDs on the reverb card. They should be lit. If the LEDs are not lit correctly then the reverb card has a problem. If the reverb card has this serious a problem that it cannot be initialized then the most likely problem is with he 56301 and associated circuitry.

If the cards are all recognized then the diagnostics can be run. There are 10 sets of diagnostic scripts available with the 960L. In addition custom scripts can be written and run from the floppy drive. The 10 built-in scripts are run by pressing the numbered button corresponding to the script desired to be run and then pressing the ENTER button. For a description of the scripts and their operation see the section labeled Functional Diagnostic test Scripts.

Audio I/O Algorithm (8 In - 8 Out):

The audio data must be generated from an external source, such as an Audio Precision. The audio I/O program is provided in the audio preset program with the parameters modified to produce a dry signal path. Three audio paths are tested. Analog in to digital out, (A-D), digital in to analog out, (D-A), and analog in to analog out, (A-A). Digital in to digital out, (D-D) is not tested directly during manufacturing proof of performance but is available as a troubleshooting tool to repair defective AES cards.

User Audio Testing:

The user will be processing audio through the 960L and LARC2 and a system all the time. The user will always be evaluating audio performance of the system. If the user detects a problem, the hardware diagnostics can be executed to see if the hardware is working. If, however, a problem is not detected, then if the user has the necessary equipment the Audio I/O program can be executed to see if the 960L and LARC2 versus something else in the users system is the problem.

Functional Diagnostic Test Scripts

Resident Scripts:

To perform the functional diagnostics, scripting files in ASCII text are executed. These files function like DOS batch files in that they contain the test or list of tests to be executed, one after the other. There are 10 built-in resident scripts. They are executed by pressing the corresponding numbered button on the LARC2 and then pressing the ENTER button. For example to run the script number 3, press the 3 button and then press the ENTER button. The 10 scripts that are resident with the 960L are described as follows:

Script 0: Lists the menu, displays a list of available scripts on the LARC2.
Script 1: Executes the entire set of diagnostic tests.

Script 2: Executes the MIDI Test and Serial Port 2 Test
Script 3: Executes the 56310 and Z80 to the DPRAM, (Dual Port RAM), Tests.
Script 4: Executes the Lexichip3 Tests.
Script 5: Executes the Z80 to SRAM and Z80 Wait Tests.
Script 6: Executes the TMIX Memory Tests
Script 7: Executes the Serial Audio Tests, the Octal data lines.
Script 8: Executes the I/O Card Cage Tests.
Script 9: Executes the MIDI Test

A full list of each script is included later in this chapter: A LISTING of RESIDENT SCRIPTS.

Custom Scripts:

Using a text editor, custom scripts can be made and run from the floppy drive. In order to perform this use a computer and type the diagnostic tests to be executed using a text editor following the syntax as outlined in the test description sections. Save the custom script with a file name. Prior to powering on the 906L connect a PS/2 compatible keyboard into the PS/2 keyboard connection on the rear of the LARC2. Power on the 960L and enter the diagnostic mode. This is performed by pressing together and holding for 2 seconds the PROGRAM and MACHINE buttons on the LARC2 immediately after powering on the 960L. The LARC2 will display Requesting Menu Mode from 960L. See the previous section 960L Diagnostic User Interface for more information. The floppy containing the custom script can be inserted into the floppy drive of the 960L at any time. After the diagnostics have been entered using the keyboard connected to the LARC2 type the command

Script [space] *a:\filename*

Where *filename* is the name of the custom script that has been created. The a:\ show the 960L the path to the custom script, where the script is located so it can find the script. This assumes the custom is in the root drive on the floppy. Don't forget to put a space between the command script and the filename.

960L Setup for Functional Diagnostic Tests

MIDI Test:

To pass the MIDI test connect a 5 Pin DIN to 5 Pin DIN cable, (MIDI cable), from the MIDI In connector to the MIDI Out connector on the I/O Clock card. In addition there are two methods to verify that the MIDI THRU connector is functioning. The first method is to connect a 5 Pin DIN to BNC cable from the MIDI THRU connector on the I/O Clock card to the input of a dual channel oscilloscope and observe the MIDI data when executing the test. Second connect the MIDI THRU port to a MIDI reader such as a PC running a MIDI terminal program, and observe the MIDI data C0 00. C0 00 is the MIDI data that is sent in the MIDI diagnostic test.

Serial Port 2 Test:

To pass the serial port 2 test connect a D9 male connector that is wired as specified later in this chapter to the REMOTE 2 connector on the I/O Clock Card. The REMOTE 1 connector is tested by communicating with a LARC2.

960L Power On Diagnostic Descriptions:

The 960L power on diagnostics are executed every time the 960L chassis is powered on. The reverb card is minimally checked for correct operation by the 960L application and the cards in the I/O cage are identified. The minimal checking of the reverb card is for time purposes. To fully verify the reverb card diagnostically the time required is approximately 20 minutes. This is unacceptably long each and every time the 960L is powered on. The results of the power on diagnostics are not displayed on the LARC2. The only method to verify that the minimal operation of the reverb card is to observe the Reverb card LEDs for

correct operation. The reverb card has 8 LEDs along the front left edge on the side of the card that faces the NLX motherboard, when the card is observed mounted in the 960L chassis. When powering on the 960L and executing the 960L application, (allow it to boot to normal operating mode), the LEDs will initially be off for about 1 minute 45 seconds. Then all the LEDs will be lit very quickly. After that the 4 leftmost LEDs, D1-D4, that are labeled Z80 #2, Z80 #2, Z80 #1, and Z80#1 respectively, will light in a periodic pattern where D1 and D4 the two outside LEDs will be on and the other two off and then D2 and D3 the two inside LEDs will be lit and the two outside LEDs will be off. This pattern will occur 4 times and take about 7 seconds. Then all four leftmost LEDs D1-D4 will be all lit for about 5 seconds. Finally the five leftmost LEDs D1-D5, where D5 is labeled SYSTEM OK will be lit, and the process is completed. The total time to perform the entire operation takes approximately 2 minutes.

The NLX motherboard has beeping that assists the technician. The first beeping occurs at 13 seconds and is 2 quick beeps to indicate no keyboard is present. The you will hear floppy drive and CD-ROM motor activity. The second beep occurs at 21 seconds and is 1 beep to indicate the BIOS is completed loading and the operating system is beginning execution. If no beeps or any other beeping pattern occurs the motherboard is not booting properly and a system level failure has occurred.

In the event of a failure the first thing to check is the power supplies. After that the motherboard is suspect and should be swapped out with a known good motherboard. Extreme care should be exercised when changing a motherboard. The bottom of the motherboard must never be allowed to come into contact with the metal chassis of the 960L. The motherboard contains a lithium battery with a thru-hole battery holder. If the leads of the battery holder come into contact with the metal chassis the battery will be shorted out and permanent damage can occur. Also the amount of force required to insert the NLX motherboard into the NLX connector is considerable. The contact pins are small and it is very easy to misalign the pins in the connector or not fully seat the motherboard giving rise to false failures. To ensure fully seating the motherboard verify that the right notched edge of the motherboard is almost against the NLX connector on the NLX backplane and that the threaded standoffs in the front of the chassis are up against the slot cutout of the motherboard support bracket.

If the 960L still won’t boot and the power supplies are good and a known good motherboard is installed correctly, the next thing to verify is the reverb card. After that verify the CD-ROM, hard disk drive, and floppy drive are working.

960L Functional Diagnostic Descriptions:

NOTE – The nomenclature for the four Lexichip3s on the reverb card will be Lexichip3 followed by a space and then the number of the Lexchip3.

The 960L functional diagnostics verify that the 960L can pass MIDI data from the Out to In ports, the two serial ports function, most of the reverb card functions, and the cards in the I/O cage can read and write to registers on their respective FPGA’s or CPLD. The following sections describe the diagnostic tests available. The syntax for the diagnostics is listed in the first line. For troubleshooting purposes a PS/2 keyboard can be connected to the LARC2 prior to powering on the 960L and individual diagnostic tests can be executed any number of times by typing the diagnostic test name followed with the optional number of times desired. A 0 entered means to run the test forever until a key is pressed on the keyboard. If no number is entered the test runs once and stops. This is the default version. The default version of all the following tests are executed by running the complete system script, which is number 1.

In order to access executing individual tests the correct path to where sets of test are located must be entered on the keyboard. The following directories/folders exist:

MIDI Tests:	The MIDI tests reside in a directory called MIDI.
Reverb Card Tests:	The reverb card tests reside in a directory called reverbcardtests.
Serial Port Tests:	The serial port tests reside in a directory called serial.
I/O Card Cage Tests:	The I/O card tests are in directory called IOBackPlane

In order to run an individual diagnostic test a keyboard must be connected to the LARC2 and the path typed on the keyboard. To get to the MIDI tests type the word MIDI after the command prompt, which is the >, (greater than symbol), and then ENTER. The commands are case insensitive. To get back to the root directory type the command cd .., which is the DOS command for change directory followed by a space then the period two times, and the ENTER. To get to the reverb card tests type reverbcardtests, all one word with no spaces, and then press ENTER. Once you are in the desired directory typing help and then pressing ENTER will provide a listing of the available tests. To see a description of any particular test type more help then the name of the test. For example to see a description of the dual port ram test, first go the directory where the test resides, reverbcardtests then press ENTER. Then type, more help dpramtest, followed by ENTER, and a description of the dual port ram test will be displayed on the LARC2.

MIDI Test:

The syntax for the MIDI test is: *MIDITest [optional NumRepeats]*.

The 960L MIDI tests verify the MIDI In to MIDI Out path. The MIDI pattern 0xC0 0x00 is generated by the 960L and sent to the MIDI Out port. Using a 5 pin DIN to 5 pin DIN cable connected from the MIDI In to MIDI Out port the C0 00 data pattern is read and the test passes. This command sends a program change message on MIDI channel 1 for program 1 (0xC0 0x00) then waits a short period for it to come back. The test reports if no data is received, if the status byte is incorrect or if the data byte is incorrect.

Optionally, a decimal number can be entered on the command line to repeat the test. When this is done, the error messages are held off until the last test try. The count is a "long" variable so the test can be repeated literally millions of times for scope loop testing. A value of 0 runs the test infinitely.

Serial Port Test:

The syntax for the serial test is: *SerialTest PortNum [optional NumRepeats]*.

Where PortNum is the port number. Ports 1 and 2 are available. Port 1 is the D9 connector labeled Remote 1 on the I/O Clock card and port 2 is labeled Remote 2. The default configuration is that Port 1 is enabled for LARC2 operation and Port 2 is enabled for serial testing. So the serial Port1 test will fail and the serial port 2 test will pass if the circuit is functioning. The system test all script, script number 1, only tests serial port2.

This test performs a test of the serial ports of the 960L. This command tests the currently selected serial port. The test sends the hex values 00, FF, 55 and AA out the designated port (TxD) and attempts to read them back (RxD). The port settings can be set in the Global Settings under the Help menu. If Terminal mode is enabled the diagnostic serial tests will fail. The terminal mode is for LARC2 communication with the 960L. The default settings are for terminal mode or LARC2 communication on port 1 and serial test enabled on port 2.

An optional "NumRepeats" value can be entered on the command line. When this is done, the test is repeated that number of times before reporting an error. A value of 0 repeats infinitely. This can be useful for debugging serial port problems.

Reverb Card Tests:

The reverb card tests consist of testing the various parts of the reverb card. These are the 56301, the 56301 to Z80 DPRAM (Dual Port RAM), the 2 Z80s, the Z80 SRAM (static RAM), the 4 Lexichip3s, and the 3 TMIX chips.

56301 Tests:

The following reverb card tests check the 56301 DSP PCI Interface chip.

56301 DPRAM Test:

The syntax for the 56301 to dual port RAM test is: *DPRAMTest CardId Z80ID [NumRepeats]*.

Tests the Dual Port RAM, associated with a specific Z80, via the 56301 This command performs a memory test on the dual port RAM (DPRAM) associated with a particular Z80 on a particular reverb card. Values of 0, 0xFF, 0xAA and 0x55 are written to the DPRAM via the 56301 then read back and confirmed An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...). This test confirms that the 56301 can access all of the DPRAM memory.

If this test fails, there is a problem with the address, data, or control lines between the 56301 and the DPRAM.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which DPRAM associated with a particular Z80 on the card to test. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

56301 to Z80 Test:

The syntax for the 56301 to Z80 test is: *56kToZ80CmdTest CardId Z80ID [NumRepeats].*

Tests the 56301's ability to notify the Z80 of a command.
This command tests the ability of the 56301 to notify the Z80 of a new command. The 56301 processor sends messages to the Z80s through the DPRAM. The DPRAMs have a special feature that facilitates this; the last two addresses of the DPRAM trigger the INT pins when written to. When address 7FE is written to from the right (56301) side, the INTL pin goes low. If the Z80 then writes to the same address, the line returns high. If the Z80 writes to address 7FF, the INTR pin goes low. If the 56301 then writes to the same address, the line returns high.

The 56301 writes data to address 7FE of the DPRAM driving the INTL line low. The INTL line feeds pin 54 (M_R) of the Lexichip3, which can then be read (via the Lexichip3) by the Z80. Before any of this, however, a tiny program is loaded into the DPRAM for the Z80 to run, which has the Z80 constantly reading address 0x3B18 in the Lexichip3 and checking for a low on bit 6 of the data it gets back. Address 0x3B18 is the location in the Lexichip3 in which the INTL pin's state is stored at bit 6. When bit 6 goes low, the program writes 0xAA into address 0x0014 of the DPRAM which the 56301 reads to confirm that the message was received. If the value at address 0x0014 of the DPRAM is not 0xAA, then the Z80 did not detect a message from the 56301 and the test fails.

In order for this test to pass, the INTL line must be connected to pin 54 of the Lexichip3. The Z80 must also be able to read from the Lexichip3's memory so the address and data lines between the Z80 and the Lexichip3 must be intact. Obviously, the mechanism within the DPRAM that triggers the INTL line going low must be functional for the test to pass.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which DPRAM associated with a particular Z80 on the card to test. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
The following tests must pass before using this test:
56301DpramTest
Z80BootTest
Z80DpramTest

Z80 Tests:

Z80 Boot Test:

The syntax for the Z80 Boot Test is: *Z80BootTest CardId Z80ID [NumRepeats]*.

This tests the Z80's ability to execute code from the DPRAM This command resets the Z80, loads a small piece of code into the dual port RAM (DPRAM) then checks to see if the Z80 program ran. The program first disables the interrupts then writes the number 0xAA to address 0x000C in the DPRAM. Finally, the Z80 halts. The diagnostic program then reads the contents of address 0x000C and confirms that it is 0xAA. This test confirms that the Z80 data bus between to the DPRAM is in tack and that at least the first 4 bits of the address bus are good as well. As a minimum, the remaining address bits must be low (but they could well be shorted). This test also confirms that the chip select, read and write lines to from the Z80 are making it to the DPRAM.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which Z80 on the card to test. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
- This test explicitly does NOT make use of the interrupt command lines (INTL, INTR).
- - It is assumed that the DPRAM Test, which accesses the DPRAM from the 56301 side, passes.

Z80 DPRAM Test:

The syntax for the Z80 DPRAM Test is: *Z80DpramTest CardId Z80ID [NumRepeats].*

Tests a Dual Port RAM (via a Z80). This test confirms that the Z80 can access most memory locations in the DPRAM. The special command trigger addresses 0x03FE and 0x03FF (0x07FE and 0x07FF in Rev 1 and higher cards) are not checked by this test. This test basically confirms that programs can safely be loaded into the DPRAM for the Z80 to run. This command loads a small piece of code into the dual port RAM (DPRAM) which writes a data value into a memory location then halts. To perform the test, the data and address values in the tiny Z80 program are modified repeatedly to fill the DPRAM with specific data which the PC reads back via the 56301 (side of the DPRAM) and checks. Values of 0, 0xFF, 0xAA, and 0x55 are tested. An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...). If this test fails but the Z80BootTest passes, there is probably a problem with the hi address lines between the Z80 and the DPRAM.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:

This specifies which Z80 on the card to reset. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
This test explicitly does NOT make use of the interrupt command lines (INTL, INTR).
It is assumed that the DPRAM Test, which accesses the DPRAM from the 56301 side, passes.

Z80 to 56301 Tests:

The syntax for the Z80 to 56301 Test is: *Z80To56kCmdTest CardId Z80ID [NumRepeats]*.

Tests the Z80's ability to notify the 56301 of a command This command tests the ability of the Z80 to notify the 56301 of a new command. The 56301 processor sends messages to the Z80s, and the Z80s send messages to the 56301 through the DPRAM. The DPRAMs have a special feature that facilitates this; the last two addresses of the DPRAM trigger the INT pins when written to. When address 7FE is written to from the right (56301) side, the INTL pin goes low. If the Z80 then writes to the same address, the line returns high. If the Z80 writes to address 7FF, the INTR pin goes low. If the 56301 then writes to the same address, the line returns high. The Z80 writes data to address 7FF of the DPRAM driving the INTR line low. The INTR line feeds the interrupt pins of the 56301. The test resets the Z80, then loads a tiny Z80 program into the beginning of the DPRAM. The Z80 program writes to DPRAM address 7FF, which pulls the INTR pin of the DPRAM low triggering an interrupt on the 56301, then halts. After loading the program into the DPRAM, the PC releases the reset on the Z80 allowing the program to run. The PC then continuously checks a memory location in the 56301 for a particular bit to be set indicating that a Z80 interrupt has occurred. As soon as the PC detects the bit, it clears it, instructs the 56301 to write to address 7FF on the DPRAM to clear the INTR pin and reports the test as passed. If the bit never goes high, the PC eventually times out and an error is reported.

In order for this test to pass, the INTR line must be connected to the buffer feeding the interrupt pins of the 56301. The Z80 must be able to access the DPRAM memory and run programs, and the mechanism within the DPRAM that triggers the INTR line going low must be functional for the test to pass.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which Z80 on the card to test. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
- The following tests must pass before using this test:
- 56301DpramTest
- Z80BootTest
- Z80DpramTest

Z80 SRAM Test:

The syntax for the Z80 SRAM Test is: *Z80SramTest CardId Z80ID [NumRepeats]*.

Tests the Z80's SRAM and the Z80's ability to access it. This command loads alternately loads two small programs into the DPRAM for the Z80, which move data to (write) and from (read) Z80 memory space. The test begins by filling the memory space under test with a specific data value then reading back the contents of each memory location, confirming the data contained therein is correct. Values of 0, 0xFF, 0xAA, and

0x55 are tested. An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...). This test confirms that the Z80 can access all of its banked SRAM.

If this test fails but the Z80BootTest and Z80DpramTest pass, there is probably a problem with the address, data or control lines between the SRAM and the Z80.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which Z80 on the card to test. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
- It is assumed that the following tests pass:
- DPRAM Test
- Z80BootTest
- Z80DpramTest

Z80 Wait Test:

The syntax for the Z80 Wait Test is: *Z80WaitTest CardId Z80ID [NumRepeats].*

This test verifies the WAIT line from the Lexichip3 to the Z80.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which Z80 on the card to reset. Legal Values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Lexichip3 Tests:

Lexichip3 WCS Test:

The syntax for the Lexichip3 WCS Test is: *Lexichip3WCSTest CardId Z80ID Lexichip3Id [NumRepeats]*.

This is a memory test of the WCS (program) memory on the Lexichip3. This test confirms that the Z80 can access all of the Lexichip3's WCS (program) memory space. The test begins by filling the memory space under test with a specific data value then reading back the contents of each memory location, confirming the data contained therein is correct. Values of 0, 0xFF, 0xAA, and 0x55 are tested. An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...).

If this test fails but the Z80BootTest and Z80DpramTest pass, there is probably a problem with the address, data or control lines between the Lexichip3 and the Z80.

Parameters:

CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Z80Id:
This specifies which Z80 on the card associated with a pair of Lexichip3's to test. Legal Values are 0 and 1.
Lexichip3Id:
This specifies which Lexichip3 associated with a particular Z80 to test. Legal values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
- It is assumed that the following tests pass:
- DPRAM Test
- Z80BootTest
- Z80DpramTest

Details:
This command alternately loads two small programs into the DPRAM for the Z80, which move data to (write), and from (read) Z80 memory space.

Lexichip3 ADF Test:

The syntax for the Lexichip3 ADF Test is: *Lexichip3ADFTest CardId Lexichip3Id [NumRepeats]*.

This tests the ADF (Audio Data File) memory on the Lexichip3. The test begins by filling the ADF memory with a specific data value then reading back the contents of each memory location, confirming the data contained therein is correct. Values of 0, 0xFFFFFF, 0xAAAAAA and 0x555555 are tested.
This test confirms that the Z80 can access all of the Lexichip3's ADF memory space and that the memory itself is operational.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
Lexichip3Id:
This specifies which Lexichip3 to test. Legal values are 0 and 1.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Notes:
- It is assumed that the following tests pass:
- DPRAM Test
- Z80BootTest
- Z80DpramTest
- Lexichip3 WCS Test

Details:
This command alternately loads two small programs into the DPRAM for the Z80, which move data to (write), and from (read) Z80 memory space. Data is written into the ADF through direct memory "writes" to the Lexichip3 but read back using the "Host Wide Data Latch".

TMIX Tests:

The following TMIX tests verify the operation of the 3 TMIX chips on the Reverb card.

TMIX Host Test:

The syntax for the TMIX Host Port Test is: *TMixHostPortTest CardId TMixID [NumRepeats]*.

This tests the 56301's ability to access a TMix's host port. This test confirms that the 56301 fully access the host port on specified TMix chip. This command writes a walking 1's pattern (0000 00001, 0000 0010, etc..) to the "Test Control Register" (address 0x7B) on the specified TMix chip. Each value is written to the register then read back and confirmed before moving on to the next value. While the data path is fully tested, the test makes no attempt to confirm that it is writing to/reading from the correct register in the TMix. Writing to the host port (and therefor a Host Register) involves writing the address of the selected Host Register to the TMix's "Pointer Port". The actual data is then written to the "Data Port" which the TMix writes to the appropriate Host Register using the address in the Pointer Port. Confirming that the Pointer Port is working properly would require setting specific Host Registers then checking to make sure that the TMix operating mode changed appropriately.

The Host Ports on the three TMIX's in the system are at the following addresses in 56301 memory space:
TMix 1:
Pointer Port - 0x9D2000
Data Port - 0x9D2001
TMix 2:
Pointer Port - 0x9D3000
Data Port - 0x9D3001
TMix 3:
Pointer Port - 0x9D4000
Data Port - 0x9D4001

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
TMixId:
This specifies which TMix on the card to test. Legal Values are 0, 1, and 2.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

TMIX DSP RAM Test:

The syntax for the TMIX DSP RAM Test is: *TMixDspRamTest CardId TMixID [NumRepeats]*.

This tests the 56301's ability to access the DPRAM in a TMIX chip The test begins by filling the memory space under test with a specific data value then reading back the contents of each memory location, confirming the data contained therein is correct. Values of 0, 0xFFFFFF, 0xAAAAAA and 0x555555 are tested. An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...).
This test confirms that the 56301 can access all of the Dual Port RAM.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
TMixId:
This specifies which TMIX on the card to test. Legal Values are 0, 1, and 2.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

TMIX Ping Pong RAM Test:

The syntax for the TMIX Ping Pong RAM Test is :*TMixPingPongRamTest CardId TMixID [NumRepeats]*.

This tests a TMix's Ping Pong RAM In addition to testing the TMIX memory itself, this test also checks the 56301's ability to access the Ping Pong RAM in a TMIX chip. The test begins by filling the memory space under test with a specific data value then reading back the contents of each memory location, confirming the data contained therein is correct. Values of 0, 0xFFFFFF, 0xAAAAAA and 0x555555 are tested. An address test is also run that writes each address value into its associated memory location (address 29 has the value 29 written into it, address 30 has the value 30 written into it, etc...).

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
TMixId:
This specifies which TMIX on the card to test. Legal Values are 0, 1, and 2.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Serial Audio Tests:

The syntax for the Serial Audio Test is: *SerialAudioTest CardID [NumRepeats]*.

This tests serial audio paths in the system. The number 555555 hex is written to each channel on each octal serial line between devices in the system. The following lines are tested:

- - TMIX 3 to Lexichip3 1
- - TMIX 3 to Lexichip3 2
- - TMIX 3 to Lexichip3 3
- - TMIX 3 to Lexichip3 4
- - Lexichip3 1 to TMIX 3
- - Lexichip3 2 to TMIX 3
- - Lexichip3 3 to TMIX 3
- - Lexichip3 4 to TMIX 3
- - Lexichip3 1 to Lexichip3 2 and Lexichip3 2 to Lexichip3 1
- - Lexichip3 3 to Lexichip3 4 and Lexichip3 4 to Lexichip3 3
- - TMIX 2 port 8 to TMIX 1 port 2 through the AES card
- - TMIX 2 port 9 to TMIX 1 port 3 through the AES card
- - TMIX 2 port 2 to TMIX 1 port 10 through the AES card
- - TMIX 2 port 3 to TMIX 1 port 0 through the AES card
- - TMIX 2 port 10 to TMIX 1 port 11 through the AES card
- - TMIX 2 port 11 to TMIX 1 port 1 through the AES card

Note that the data is shifted 1 bit to the right when it passes through the AES card (in its loopback mode) so data is reported as 2AAAAA for tests, which use it.

Parameters:
CardID:
This number selects which reverb card to test. Legal values are 0 and 1, since only two reverb cards will be supported. If only one card is present use the number 0.
NumRepeats:
This optional parameter specifies how many times to run the test. A value of 0 runs the test indefinitely (until a key is pressed). Dots are shown on the display to indicate that the test is still running.

Devices:
0 - TMIX 1

1 - TMIX 2
2 - TMIX 3
3 – Lexichip3 1
4 – Lexichip3 2
5 – Lexichip3 3
6 – Lexichip3 4

Device Port Assignments:

TMIX 1 (DeviceID: 0): Interfaces with the IO backplane. Typically used for inputs.
0 - TMIX_1_SERD0
1 - TMIX_1_SERD1
2 - TMIX_1_SERD2
3 - TMIX_1_SERD3
4 - TMIX_1_SERD4
5 - TMIX_1_SERD5
6 - TMIX_1_SERD6
7 - TMIX_1_SERD7
8 - TMIX_1_SERD8
9 - TMIX_1_SERD9
10 - TMIX_1_SERD10
11 - TMIX_1_SERD11

TMIX 2 (DeviceID: 1): Interfaces with the IO backplane. Typically used for outputs.
0 - TMIX_2_SERD0
1 - TMIX_2_SERD1
2 - TMIX_2_SERD2
3 - TMIX_2_SERD3
4 - TMIX_2_SERD4
5 - TMIX_2_SERD5
6 - TMIX_2_SERD6
7 - TMIX_2_SERD7
8 - TMIX_2_SERD8
9 - TMIX_2_SERD9
10 - TMIX_2_SERD10
11 - TMIX_2_SERD11

TMix 3 (DeviceID: 2)
0 - LEXI_1_SER_IN (Output to Lexichip3 port 0)
1 - LEXI_2_SER_IN (Output to Lexichip3 port 0)
2 - LEXI_3_SER_IN (Output to Lexichip3 port 0)
3 - LEXI_4_SER_IN (Output to Lexichip3 port 0)
4 - LEXI_1_SER_OUT (Input from Lexichip3 port 0)
5 - LEXI_2_SER_OUT (Input from Lexichip3 port 0)
6 - LEXI_3_SER_OUT (Input from Lexichip3 port 0)
7 - LEXI_4_SER_OUT (Input from Lexichip3 port 0)

Lexichip3 1 (DeviceID: 3)
0 - Input: LEXI_1_SER_IN (from TMIX **3** port **0**)
0 - Output LEXI_1_SER_OUT (to TMIX **3** port **4**)
1 - Input: LEXI2_TO_LEXI1_SER (from Lexichip3 **2** port **1**)
1 - Output LEXI1_TO_LEXI2_SER (to Lexichip3 **2** port **1**)

Lexichip3 2 (DeviceID: 4)
0 - Input: LEXI_2_SER_IN (from TMIX **3** port **1**)
0 - Output LEXI_2_SER_OUT (to TMIX **3** port **5**)
1 - Input: LEXI1_TO_LEXI2_SER (from Lexichip3 **1** port **1**)
1 - Output LEXI2_TO_LEXI1_SER (to Lexichip3 **1** port **1**)

Lexichip 3 (DeviceID: 5)
0 - Input: LEXI_3_SER_IN (from TMIX **3** port **2**)
0 - Output LEXI_3_SER_OUT (to TMIX **3** port **6**)
1 - Input: LEXI4_TO_LEXI3_SER (from Lexichip3 **4** port **1**)
1 - Output LEXI3_TO_LEXI4_SER (to Lexichip3 **4** port **1**)

Lexichip3 4 (DeviceID: 6)
0 - Input: LEXI_4_SER_IN (from TMIX **3** port **3**)
0 - Output LEXI_4_SER_OUT (to TMIX **3** port **7**)
1 - Input: LEXI3_TO_LEXI4_SER (from Lexichip3 **3** port **1**)
1 - Output LEXI4_TO_LEXI3_SER (to Lexichip3 **3** port **1**)

Notes:
- It is assumed that the following tests pass:
- DPRAM Test
- Z80BootTest
- Z80DpramTest
- LexichipWCSTest

I/O card Tests:

The following tests verify communication with the cards in the I/O Cage. These are the I/O Clock, Analog In, Analog Out and AES cards.

I/O Clock card Test:

The syntax for the I/O Clock card test is: *IOClockBdTest CardID [optional NumRepeats]*.

This tests the control interface to the IO Clock card This command writes a walking 1s pattern to the control register on the IO backplane's Clock card, reading the data back to confirm it.

Card Id:
This defines which card in the system to access. Initial systems will only contain a single card so a value of 0 should be used. An additional card would use a value of 1.
NumRepeats: (optional)
This defines how many times the test is run. The default (if not entered) is 1 time. A value of 0 runs the test infinitely. Pressing any key exits the loop.

Analog Input card Test:

The syntax for the Analog Input card Test is: *IOAInBdTest CardID [optional NumRepeats]*.

This tests the control interface to the Analog Input card This command writes a walking 1s pattern to the control register on the IO backplane's Analog In card, reading the data back to confirm it.

Card Id:
This defines which card in the system to access. Initial systems will only contain a single card so a value of 0 should be used. An additional card would use a value of 1.
NumRepeats: (optional)
This defines how many times the test is run. The default (if not entered) is 1 time. A value of 0 runs the test infinitely. Pressing any key exits the loop.

Analog Output card Test:

The syntax for the Analog Output card test is: *IOAOutBdTest CardID [optional NumRepeats]*.

This tests the control interface to the Analog Output card This command writes a walking 1s pattern to the control register on the IO backplane's Analog Output card, reading the data back to confirm it.

Card Id:
This defines which card in the system to access. Initial systems will only contain a single card so a value of 0 should be used. An additional card would use a value of 1.
NumRepeats: (optional)
This defines how many times the test is run. The default (if not entered) is 1 time. A value of 0 runs the test infinitely. Pressing any key exits the loop.

AES card Test:

The syntax for the AES card Test is: *IOAESBdTest CardID [optional NumRepeats]*.

This tests the control interface to the AES card This command writes a walking 1s pattern to the control register (offset 0x20) on the IO backplane's AES card, reading the data back to confirm it.

Card Id:
This defines which card in the system to access. Initial systems will only contain a single card so a value of 0 should be used. An additional card would use a value of 1.
NumRepeats: (optional)
This defines how many times the test is run. The default (if not entered) is 1 time. A value of 0 runs the test infinitely. Pressing any key exits the loop.

960L Troubleshooting Tools:

As outlined in the sections on Functional Diagnostic Test Scripts and in the Functional Diagnostic Descriptions custom test scripts can be implemented and individual tests can be performed to troubleshoot defective 960Ls. In order to perform these actions a PS/2 keyboard must be connected to the LARC2 prior to powering on the 960L. See these sections for information on how to use the keyboard to perform these functions.

MIDI Troubleshooting Tool:

MIDI Send:

The syntax to send MIDI data is: *MIDISend (data).*

This tool outputs MIDI General MIDI messages. This command sends data to the MIDI output device. Currently, only general MIDI messages are supported (no SysEx).

NOTE - "Data" must be in the hex format.
Example:
MIDISend C0 00
Sends a MIDI program change message on channel 1 for program 1 (0).

MIDI Information:

The syntax to get MIDI information is: *MIDIInfo (no parameters).*

This tool displays information about MIDI devices in the system. This command displays information about the MIDI devices in the system. It takes about a second to process the command.

Serial Port Troubleshooting Tools:

Send Serial Data:

The syntax to send serial data is: *SerialSend [data]*.

This tool sends serial data bytes out the serial port This is a debugging tool that allows data to be sent out the serial port. Up to 15 bytes can be sent at a time.

Set the Serial Port:

The syntax to set the serial port is: *SerialSetPort [port num]*.

This tool sets the active serial port or reports the current selection. This command sets the serial port that will be used by the diagnostic commands. If executed with no parameters, the currently selected serial port is reported.

Parameters:
Legal values for the port num are 1 and 2.

Note that the SerialSetPort cannot be run if the "Terminal" is enabled. Terminal mode is the default for Port 1 due to the LARC2 using this port.

Global Commands:

TimeDate:

Displays the current time and date
This command is typically used in script files to provide a timestamp, which will appear in a log file. This can be examined later to determine when the test was run (before or after repairs were made, for instance).

Version:

Reports the current version of the diagnostics.
Prints the current version on the display or log file along with date and time the software was created.

Rem [text]:

Allows comments to be added to script files. The Rem (remark) command allows comments to be added to script files. The command itself actually does nothing.

Echo:

Echo followed by a message prints messages to the screen/log file. The echo command allows messages to be printed on the display. Though it will operate directly from the command line, Echo was really added to provide documentation and feedback from script files. Up to 16 words 32 characters long can be used

Script:

The script command followed by a complete path and filename executes commands from a script file
This command allows multiple commands or tests to be executed from a text based "script" file. Commands are entered in the file as they would be on the command line. The effect is very similar to a DOS batch file. Several commands from the DOS world have been emulated here to facilitate writing, maintaining, and using script files: Echo and Rem. Like it's DOS equivalent, Echo "echos" text following the command to display when the script is run. The Rem command basically does nothing but allows "emarks" (or comments) to be added to the script file to help document what is going on

Help:

The help command provides a list of tests available in the directory that you are in and also information about other commands.

More [HELP command]:

The More command followed by help and then a test name displays extended help for the indicated command. This displays the extended help information for the command entered on the command line after the word HELP. If no command is specified, it attempts to locate information on the previous command.

CD [parameters]:

The cd command changes the current directory level of the diagnostics. Like it's DOS equivalent, this command changes the current working directory. When executed with a directory name as a parameter, the directory is entered. When executed with ".." (without the quotes), the diagnostics go up a level (stopping at the root)

LogFile:

The logfile command opens, closes and provides information in a log file. The Log File records all displayed information from the diagnostics into a text file. This is useful for reviewing the activities of an automated script file or reporting bugs. The logfile command can also be used to acquire the serial number of a 960L.

Usage:
- When executed with no parameters, displays the current log file name.
- When executed with "ON" as a parameter, the log file is enabled (opened)
- When executed with "OFF" as a parameter, the log file is disabled (closed)
- When executed with a file name as a parameter, the new name is used for the log file. If the LogFile was already enabled, the previous file is closed and the new file is opened.
- To acquire the serial number turn the logfile off by typing logfile disabled. Then change the name of the logfile by typing logfile c:\960lserialno. Then type the command viewlog. The serial number of the 960L on the hard drive will be displayed followed by the date of manufacture. The date of manufacture is listed as a four digit number with the month being the first two and the year being the last two.

Exit

This command exits the diagnostic program.

Root

This command goes to the top of the command tree

Dir:

The dir command shows all of the commands available at the current level. This is similar to the DOS equivalent.

LISTING of RESIDENT SCRIPTS

Script 0

```
REM
REM ////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //        File: 0.htm
REM //
REM // Description: This document is a script file that runs all available tests
```

```
REM //
REM //     History: 03/13/2000  rjs Created
REM //
REM ////////////////////////////////////////////////////////////////////////
REM
help
REM
```

Script 1

```
REM
REM ////////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 1.htm
REM //
REM // Description: This document is a script file that runs all available tests
REM //
REM //     History: 03/13/2000  rjs Created
REM //              05/17/2000  clc modified to run all the system tests
REM //
REM ////////////////////////////////////////////////////////////////////////
REM
TimeDate
cd Midi
MidiTest
cd ..
cd Serial
SerialTest 2
cd ..
cd Reverbcardtests
Dpramtest 0 0
Dpramtest 0 1
Z80BootTest 0 0
Z80BootTest 0 1
Z80DpramTest 0 0
Z80DpramTest 0 1
56kToZ80CmdTest 0 0
56kToZ80CmdTest 0 1
Z80To56kCmdTest 0 0
Z80To56kCmdTest 0 1
LexichipWcsTest 0 0 0
LexichipWcsTest 0 0 1
LexichipWcsTest 0 1 0
LexichipWcsTest 0 1 1
LexichipAdfTest 0 0
LexichipAdfTest 0 1
LexichipAdfTest 0 2
LexichipAdfTest 0 3
LexichipDramTest 0 0 0
LexichipDramTest 0 0 1
LexichipDramTest 0 1 0
```

```
LexichipDramTest 0 1 1
Z80SramTest 0 0
Z80SramTest 0 1
z80waittest 0 0 0
z80waittest 0 0 1
z80waittest 0 1 0
z80waittest 0 1 1
TMIXHostPortTest 0 0
TMIXHostPortTest 0 1
TMIXHostPortTest 0 2
TMIXDspRamTest 0 0
TMIXDspRamTest 0 1
TMIXDspRamTest 0 2
TMIXPingPongRamTest 0 0
TMIXPingPongRamTest 0 1
TMIXPingPongRamTest 0 2
SerialAudioTest 0
cd ..
cd IOTools
IOClockBdTest 0
IOAInBdTest 0
IOAOutBdTest 0
IOAESBdTest 0
cd ..
REM
```

Script 2

```
REM
REM ///////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 2.htm
REM //
REM // Description: This document is a script file that runs all available tests
REM //
REM //    History: 03/13/2000  rjs Created
REM //             05/17/2000  clc modified to run the MIDI
REM //                              and Serial Tests
REM ///////////////////////////////////////////////////////////////////////
REM
cd Midi
MidiTest
cd ..
cd Serial
REM serialtest 1
serialtest 2
cd ..
REM
```

Script 3

```
REM
```

```
REM ////////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 3.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //    History: 03/13/2000  rjs Created
REM //             05/17/2000  clc modified to test the 56301 and Z80
REM //                         to the Dual Port Ram
REM ////////////////////////////////////////////////////////////////////////
REM
cd Reverbcardtests
Dpramtest 0 0
Dpramtest 0 1
Z80BootTest 0 0
Z80BootTest 0 1
Z80DpramTest 0 0
Z80DpramTest 0 1
56kToZ80CmdTest 0 0
56kToZ80CmdTest 0 1
Z80To56kCmdTest 0 0
Z80To56kCmdTest 0 1
cd ..
REM
```

Script 4

```
REM
REM ////////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 4.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //    History: 03/13/2000  rjs Created
REM //             05/17/2000  clc modified to run the Lexichip tests
REM ////////////////////////////////////////////////////////////////////////
REM
cd Reverbcardtests
LexichipWcsTest 0 0 0
LexichipWcsTest 0 0 1
LexichipWcsTest 0 1 0
LexichipWcsTest 0 1 1
LexichipAdfTest 0 0
LexichipAdfTest 0 1
LexichipAdfTest 0 2
```

```
LexichipAdfTest 0 3
LexichipDramTest 0 0 0
LexichipDramTest 0 0 1
LexichipDramTest 0 1 0
LexichipDramTest 0 1 1
cd ..
REM
```

Script 5

```
REM
REM ////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 5.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //     History: 03/13/2000  rjs Created
REM //              05/17/2000  clc modified to run the
REM //                          Z80 SRAM and Wait Tests
REM //
REM ////////////////////////////////////////////////////////////////////
REM
cd Reverbcardtests
Z80SramTest 0 0
Z80SramTest 0 1
z80waittest 0 0 0
z80waittest 0 0 1
z80waittest 0 1 0
z80waittest 0 1 1
cd ..
REM
```

Script 6

```
REM
REM ////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 6.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //     History: 03/13/2000  rjs Created
REM //              05/17/2000  clc modified to run the TMIX Tests
REM //
REM ////////////////////////////////////////////////////////////////////
```

```
REM
cd Reverbcardtests
TMIXHostPortTest 0 0
TMIXHostPortTest 0 1
TMIXHostPortTest 0 2
TMIXDspRamTest 0 0
TMIXDspRamTest 0 1
TMIXDspRamTest 0 2
TMIXPingPongRamTest 0 0
TMIXPingPongRamTest 0 1
TMIXPingPongRamTest 0 2
cd ..
REM
```

Script 7

```
REM
REM //////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 7.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //     History: 03/13/2000  rjs Created
REM //              05/17/2000  clc modified to run the Serial Audio Test
REM //////////////////////////////////////////////////////////////////////
REM
cd Reverbcardtests
SerialAudioTest 0
cd ..
REM
```

Script 8

```
REM
REM //////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 8.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //     History: 03/13/2000  rjs Created
REM //              05/17/2000  clc modified to run the IO card Tests
REM //
REM //////////////////////////////////////////////////////////////////////
REM
```

```
cd IOTools
IOClockBdTest 0
IOAInBdTest 0
IOAOutBdTest 0
IOAESBdTest 0
cd ..
REM
```

Script 9

```
REM
REM ////////////////////////////////////////////////////////////////////////
REM // 960L Diagnostics Test Script
REM //
REM // COPYRIGHT (C) 2000, LEXICON INC., ALL RIGHTS RESERVED.
REM // NO PART OF THIS DOCUMENT MAY BE REPRODUCED IN ANY FORM WITHOUT THE
REM // EXPRESSED WRITTEN PERMISSION OF LEXICON INC.
REM //
REM //       File: 9.htm
REM //
REM // Description: This document is a script file that tests the MIDI Port
REM //
REM //    History: 03/13/2000  rjs Created
REM //
REM ////////////////////////////////////////////////////////////////////////
REM
cd midi
MidiTest
cd ..
rem cd Reverbcardtests
rem SerialAudioTest 0
rem z80dpramtest 0 0
rem tmixHostPortTest 0 0
rem z80waittest 0 0
rem tmixdspramtest 0 0
rem cd Reverbcardtools
rem SerialAudioTool 0 0 0 0 555555
rem LexichipAdfTool 0 0 0 55AAFF
rem LexichipAdfTest 0 0
```

LARC2 DIAGNOSTICS

There are two categories of diagnostics that exist in the LARC2 software: 1) Power On Diagnostics, and 2) Interactive Diagnostics. The Power On Diagnostics are executed automatically when the LARC2 is first powered on. The Interactive Diagnostics are used to perform functional tests that are not performed during the Power On Diagnostics, and also for troubleshooting purposes.

There are two ways that the 'Interactive Diagnostics' menu mode can be invoked, they are as follows:

1. By installing a RS-422 Wraparound Plug in the HOST connector, then powering on the unit.

2. By pressing and holding the 'PROGRAM' + 'ENTER' keys while powering on the unit.

NOTE: Hold the 'PROGRAM' + 'ENTER' keys until a chase pattern appears on the LARC2 Main board and Meter board LED's (after approximately 8 seconds). When the chase pattern appears, release the

'PROGRAM' + 'ENTER' keys.

NOTE: There are two other modes that can also be entered during the Power On Diagnostics, they are as follows:

1. To enter the 'Option Board Menu' mode, press and hold the 'REGISTER' + 'CONTROL' keys while powering on the unit, then release the keys after approximately 8 seconds. This mode is used primarily for programming the LARC2 Boot ROM and Program Flash Memory during the manufacturing test process. Refer to the Option Board Menu section of this document for more information.

2. To enter the 'Menu' mode, press and hold the 'PROGRAM' + 'MACHINE' keys while powering on the unit. This mode is used primarily for programming the LARC2 Boot ROM and Program Flash Memory when the LARC2 is connected to a 960L mainframe. Refer to the 960L Diagnostics Descriptions document (P/N 010-13397) for more information.

Debug Port:

The text that is displayed on the LARC2 LCD display in these modes is also sent to the 'Debug' port of the LARC2 Option Board (when installed). Connecting a (RS-232) serial 'Debug' terminal to the 'Debug' port is an extremely useful tool for debugging purposes. Another advantage of using the debug terminal is that the terminal keyboard can also be used to execute the Interactive Diagnostic tests on the LARC2 when the use of the keypad is not possible or impractical.

During the Power On Diagnostics, diagnostic information is sent to the 'Debug' port of the LARC2 Option Board (when installed) which is not displayed on LARC2 LCD display as shown in the example below:

(NOTE: In the example below, a PCMCIA Ethernet Card was installed on the LARC2 Option Board, and an

External Keyboard was not connected to the LARC2 'AUX' port.

Determining boot cause.
Reset detected.
Memory Data Test
Beginning memory wipe.
Copy Rom and Enable MMU.
Copy Verified
After MMU
SP= C00AFFFC
After Stack
Running tests...

****ERR**KB08** Keyboard TimeoutReset socket 1 succeeded**
PCMGetStatus: Socket 1 GPLR = 0bdae36c
PcCard 1 is present
PcCard 1, Requesting window
Read first tuple
Checking Card Type
Card Type 6
Checking Card Type
Card Type 6

The 'Debug' terminal should be configured as follows; Baud Rate: 57600 (Bits Per Second), Data Bits: 8, Stop Bits: 1, Parity: None, Flow Control: Xon/Xoff, Terminal Emulation: ANSI.

POWER ON DIAGNOSTICS:

There are two LED's located on the LARC2 Main Board which are used for displaying the status of the Power On Diagnostic tests that are performed before the LED's on the Meter Board or LCD display are enabled. Upon normal power up, the two LED's 'MSB(1)' and 'LSB(0)' perform a binary countdown from 3 to 0 (11, 10, 01 & 00).

NOTE: There are no error messages during this portion of the Power On Diagnostics. In the event that a diagnostic failure has occurred, the system will halt on the failed test. The binary value displayed on the two LED's indicates where the failure occurred during the Power On Diagnostic test sequence.

Power On Diagnostics Sequence:

When the LARC2 is first powered on, all of the LED's on the Meter Board and Main Board (keypad) will be turned on for approximately 5 seconds, during this period the following sequence of operations are performed as the Power On Diagnostic tests are executed. These operations are all being executed from the Boot ROM.

- Initialization:

  During this operation, the SA-1100 is reset, its registers are initialized, the interrupts are disabled, and the Main Board LSB(0) and MSB(1) LED's are turned on to display the binary value of 3.

MSB(1) ON, LSB(0) ON:

- Determine Boot Cause:

  During this operation, the Boot cause is determined, which is normally because reset has been detected.

- Boot ROM Checksum:

  During this operation, the checksum of the Boot ROM is verified, and the Main Board LSB(0) LED is turned OFF to display the binary value of 2.

MSB(1) ON, LSB(0) OFF:

- Memory Test (DRAM Data Bus):

  During this operation, the DRAM Data Bus is tested by first writing 00000000 (hex) into 512 memory locations of the DRAM, then the same 512 locations are read to verify the data written in these locations is correct. The same write/read sequence is also performed using the following (hex) values: FFFFFFFF, AAAAAAAA, 55555555, CCCCCCCC, 33333333, 99999999 & 66666666.

  During the test, the DRAM data lines (SA_D0-SA_D31) are tested using the data patterns listed in the table below. Refer to the table below for the hex to binary conversion of the data patterns: FFFFFFFF, AAAAAAAA, 55555555, CCCCCCCC, 33333333, 99999999 & 66666666.

  During the test, the DRAM data lines (SA_D0-SA_D31) are tested using the data patterns listed in the table below. Refer to the table below for the hex to binary conversion of the data patterns:

HEX VALUE:	MSB BINARY CONVERSION: LSB
00000000	0000 0000 0000 0000 0000 0000 0000 0000

FFFFFFFF	1111 1111 1111 1111 1111 1111 1111 1111
AAAAAAAA	1010 1010 1010 1010 1010 1010 1010 1010
55555555	0101 0101 0101 0101 0101 0101 0101 0101
CCCCCCCC	1100 1100 1100 1100 1100 1100 1100 1100
33333333	0011 0011 0011 0011 0011 0011 0011 0011
99999999	1001 1001 1001 1001 1001 1001 1001 1001
66666666	0110 0110 0110 0110 0110 0110 0110 0110

When a DRAM Data Bus failure is encountered, the test will stop and loop continuously at the failed address location. The address where the error occurred, along with the data sent, and the data received is sent to the Debug Port.

- Memory Test (DRAM Address Bus):

During this operation, the DRAM Address Bus is tested by first writing the current address into 25 memory locations of the DRAM using 32 bit words, then the same memory locations are read to verify the data written in these locations is correct. During the test, DRAM address lines (BMA10-BMA21) are tested using the addresses listed in the table below. Refer to the table below for the hex to binary conversion of the data patterns:

HEX VALUE:	MSB BINARY CONVERSION: LSB
C0000000	1100 0000 0000 0000 0000 0000 0000 0000
C0000004	1100 0000 0000 0000 0000 0000 0000 0100
C0000008	1100 0000 0000 0000 0000 0000 0000 1000
C0000010	1100 0000 0000 0000 0000 0000 0001 0000
C0000020	1100 0000 0000 0000 0000 0000 0010 0000
C0000040	1100 0000 0000 0000 0000 0000 0100 0000
C0000080	1100 0000 0000 0000 0000 0000 1000 0000
C0000100	1100 0000 0000 0000 0000 0001 0000 0000
C0000200	1100 0000 0000 0000 0000 0010 0000 0000
C0000400	1100 0000 0000 0000 0000 0100 0000 0000
C0000800	1100 0000 0000 0000 0000 1000 0000 0000
C0001000	1100 0000 0000 0000 0001 0000 0000 0000
C0002000	1100 0000 0000 0000 0010 0000 0000 0000
C0004000	1100 0000 0000 0000 0100 0000 0000 0000
C0008000	1100 0000 0000 0000 1000 0000 0000 0000
C0010000	1100 0000 0000 0001 0000 0000 0000 0000
C0020000	1100 0000 0000 0010 0000 0000 0000 0000
C0040000	1100 0000 0000 0100 0000 0000 0000 0000
C0080000	1100 0000 0000 1000 0000 0000 0000 0000
C0100000	1100 0000 0001 0000 0000 0000 0000 0000
C0200000	1100 0000 0010 0000 0000 0000 0000 0000
C0400000	1100 0000 0100 0000 0000 0000 0000 0000
C0800000	1100 0000 1000 0000 0000 0000 0000 0000
C1000000	1100 0001 0000 0000 0000 0000 0000 0000
C2000000	1100 0010 0000 0000 0000 0000 0000 0000

When a DRAM Address Bus failure is encountered, the test will stop and loop continuously at the failed address location. The address where the error occurred, along with the data sent, and the data received is sent to the Debug Port.

NOTE: Since this test utilizes 32 bit words (4 bytes) it is not possible to test the address lines 0 & 1.

- Copy ROM to RAM:

During this operation, the Boot ROM is copied to the DRAM, then the data written to the DRAM is verified by performing a byte by byte compare with the data stored in the Boot ROM. The Main Board MSB(1) LED is turned OFF, and the LSB(0) LED is turned ON to display the binary value of 1.

MSB(1) OFF, LSB(0) ON:

- During this operation, the MMU and interrupts are enabled on the SA-1100. The Stack Pointer is initialized, and the LARC2 jumps to the (C-code) program. This is where the LARC2 begins to execute the program from the DRAM. The Serial Debug port, Keyboard 'AUX' port, and Timers (to setup the system clock) are initialized. The LCD display is turned on displaying the 'Lexicon' splash screen.

  From this point on, the software begins to continuously monitor for 'PROGRAM' + 'MACHINE' keys being pressed. If the 'PROGRAM' + 'MACHINE' key combination is detected, a flag is set for the LARC2 to enter Menu Mode upon completion of the Power On Diagnostic tests.

  The LED's on the Main Board and Meter Board are turned off. The FPGA loads its code from the Xilinx SPROM, and waits for the FPGA Done signal. The Main Board LSB(0) LED is turned OFF to display the binary value of 0.

MSB(1) OFF, LSB(0) OFF:

- During this operation, the GPIO's on the SA-1100 are enabled. The External Keyboard hardware is reset. The HOST port is initialized, and the A/D Converters are setup (values are written to registers on the SA-1100).

Power On Self Tests:

Pass/Fail Results:

From this point on, the Pass/Fail results for the Power On Diagnostic tests are displayed on the Meter Board LED's. The LED column numbers are used to indicate the number of the test (1-4 & 6-8) respectively. For example; the Pass/Fail results for Test 1 are displayed on the LED's located in column 1. The LED colors are used to indicate the Pass/Fail status of the diagnostic tests are as follows:

Red = Failed
Yellow = Undetermined
Green = Passed

NOTE: The term 'Undetermined' means the diagnostic test did not detect the presence of a device connected to the LARC2, and the associated circuitry in the LARC2 could not be tested. As a result, the diagnostic test could not determine whether the associated circuitry was good or bad.

Upon normal power up (with the PS/2 Keyboard and RS-422 Wraparound Plug installed), the Meter Board LED's will display the Power On Diagnostics test results as shown in the table below:

LED:	#1	#2	#3	#4	#5	#6	#7	#8
Red	0	0	0	0	0	0	0	0
Yellow	0	0	0	0	0	0	0	0
Green	1	1	1	1	0	1	1	1

(0=OFF, 1=ON)

When the Interactive Diagnostics are entered by holding the 'PROGRAM' + ENTER' keys during power up, without the PS/2 Keyboard and Wraparound Plug installed. The following Meter Board LED's will be turned on to indicate the three errors that have been detected, as shown in the table below:

LED:	#1	#2	#3	#4	#5	#6	#7	#8

Red	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Yellow	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
Green	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**

(0=OFF, 1=ON)

1. *The YELLOW #6 LED was turned on to indicate a Keyboard Test failure because the External Keyboard was not detected.*

2. *The YELLOW #7 LED was turned on to indicate a Loop Back Test failure because the RS-232 Wraparound Plug was not detected.*

3. *The RED #8 LED was turned on to indicate a Keystuck Test failure because the 'PROGRAM' + 'ENTER' keys were being held.*

Prior to the execution of the Power On Self Tests, the Realtime Clock is tested. This test verifies the operation of the 32.768kHz crystal on the SA-1100.

TEST 1: Motor Waveform Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 2: Motor Control Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 3: A/D Control Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 4: A/D Self Test

This test reads the MIN, MID and MAX values based on the reference voltage of the A/D converter.

TEST 5: (Not Used)

TEST 6: External PS/2 Keyboard Test

This test initializes the External Keyboard, and tests for the presence of a keyboard connected to the 'AUX' port of the LARC2 by sending 8 characters out the port, and monitors any data that is received. The data received is then compared to what was sent.

NOTE: This test requires an External Keyboard connected to the 'AUX' port. Otherwise the test will fail when an External Keyboard is not present. Diagnostic error messages are also sent to the Debug Port to indicate when a failure has occurred as shown in the example below.

****ERR**KB01** TXRDY= 0. should be 1, GPIO= fffc7ec**
****ERR**KB02** IBFULL= 1 should be 0, Stat= 12, GPIO= fffc7ec**
****ERR**KB03** Keyboard Timeout**

TEST 7: Host Port (Loop Back) Test

This test checks for the presence of a Loop Back Plug connected to the 'HOST' port of the LARC2 by sending 8 characters out the port, and monitors any data that is received. The data received is then compared to what was sent.

NOTE: This test requires a Female RS-422 Wraparound Plug installed in the 'HOST' port. Otherwise the test will fail when the Loop Back Plug is not present. A diagnostic error message is also sent to the Debug Port to indicate when a failure has occurred as shown in the example below:

Loop Back Not installed

TEST 8: Keystuck & Fader Touch Test

This test checks for keys stuck (closed) on the LARC2 Main Board, or if any of the Faders were being touched during the Power On Diagnostic tests.

- PCMCIA Card Detection:

During this operation, the Power On Diagnostics checks for presence of a PCMCIA Card installed on the Option Board, if a PCMCIA card has been detected a flag is set.

- Voltage Test:

During this operation, a voltage test is performed to verify the +12V Power Supply is operating between 10-13 volts by reading the A/D Converter value of the 12VSENSE signal.

NOTE: If a PCMCIA Card was detected during the PCMCIA Card Detection routine (above), the card is now initialized, and the card type is also detected.

⇒ If the Option Board and PCMCIA Card were present, the LARC2 will now enter the 'Option Board Menu' as shown in the example below: *(Refer to the Option Board Menu section of this document for more information.)*

NOTE: The top line of the 'Interactive Diagnostics' menu displays the date and time of the Boot ROM build, and line 2 displays the Boot ROM version (the actual text may vary).

```
*      LARC2 Menu file built Apr 11 2000, 14:52:36    *
* Bootrom Version 0.13
**********************************************************


 1]   Display Register                         X]   Download via XModem
 2]   Set Register                             F]   Flash Operations
 3]   Dump Memory                              K]   Keyboard Echo
 4]   Set Memory                               D]   Interactive Diagnostics
 5]   Erase FLASH                              I]   Enable Interrupts
 7]   Display Ethernet Information             L]   Loop on read
 8]   Set Up Ethernet Information              S]   Diagnostics Suite
 9]   Download Image Via Ethernet(ESHELL)      Z]   ZModem Download
 A]   Load from PCMCIA Flash                   O]   Option-Board Test
 B]   Boot @ d0000000
 C]   Fill Memory with a Pattern
```

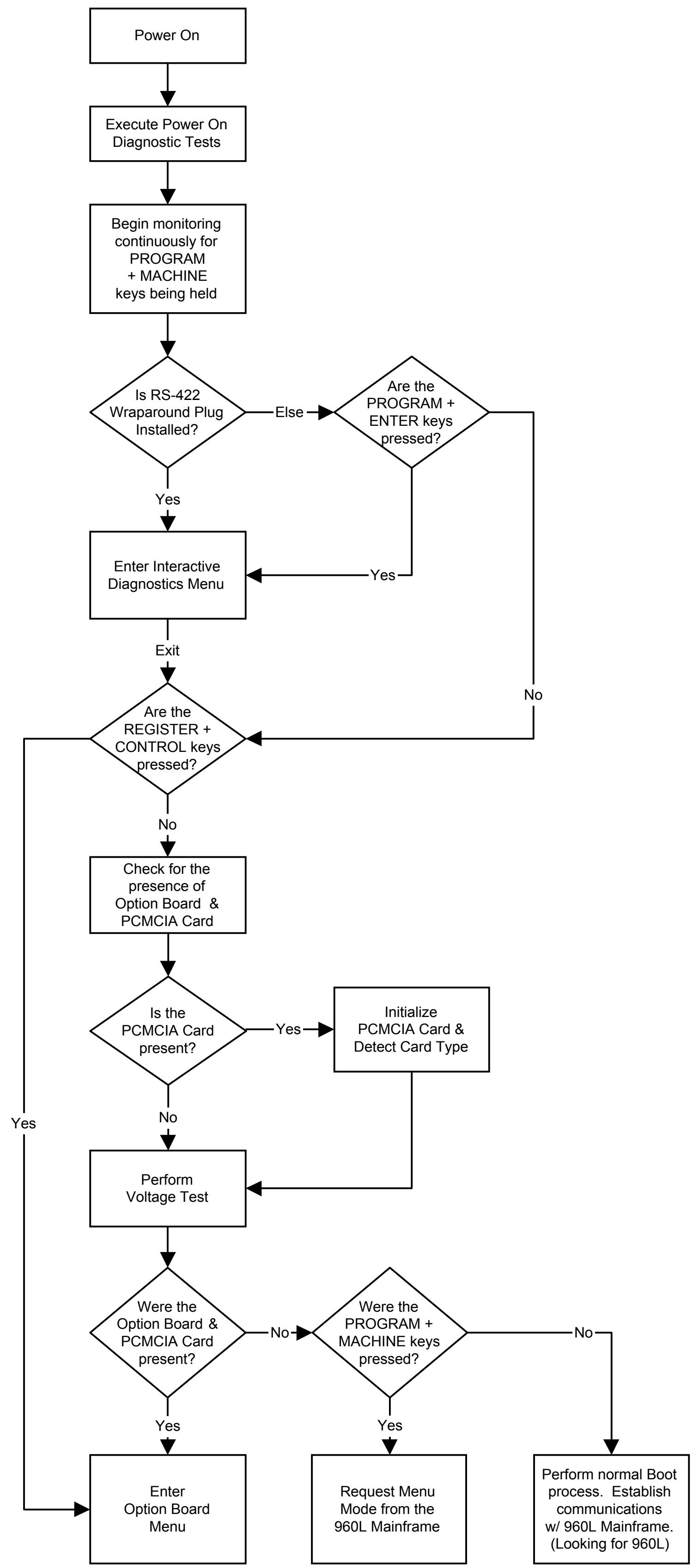
⇒ If the 'PROGRAM' + 'MACHINE' keys were pressed during the Power On Diagnostics, the LARC2 will now request the Menu mode from the 960L Mainframe (when the LARC2 is connected to a 960L). The LCD display on the LARC2 will indicate the following:

Requesting Menu Mode from 960L...

⇒ If the 'PROGRAM' + 'MACHINE' keys were not pressed during the Power On Diagnostics, the LARC2 will now perform a normal boot process, and attempt to establish communications with the 960L Mainframe (when the LARC2 is connected to a 960L). The LCD display on the LARC2 will indicate the following:

Looking for 960L...

For detailed information on the Power On Diagnostics & Boot Sequence refer to the flowchart below:


Power On
Execute Power On Diagnostic Tests
Begin monitoring continuously for PROGRAM + MACHINE keys being held
Is RS-422 Wraparound Plug Installed?
Else
Are the PROGRAM + ENTER keys pressed?
Yes
Enter Interactive Diagnostics Menu
Yes
Exit
No
Are the REGISTER + CONTROL keys pressed?
No
Check for the presence of Option Board & PCMCIA Card
Is the PCMCIA Card present?
Yes
Initialize PCMCIA Card & Detect Card Type
Yes
No
Perform Voltage Test
Were the Option Board & PCMCIA Card present?
No
Were the PROGRAM + MACHINE keys pressed?
No
Yes
Yes
Enter Option Board Menu
Request Menu Mode from the 960L Mainframe
Perform normal Boot process. Establish communications w/ 960L Mainframe. (Looking for 960L)

INTERACTIVE DIAGNOSTICS:

The following section describes the operation of the Interactive Diagnostic Tests.

There are two ways that the 'Interactive Diagnostics' menu mode can be invoked, they are as follows:

1. Press & hold the 'PROGRAM' + 'ENTER' keys while powering on the LARC2, then releasing the 'PROGRAM' + 'ENTER' keys when a chase pattern appears on the Meter Board and Keypad LED's.

2. Install the Female RS-422 Wraparound (Loop Back) Plug into the connector labeled 'HOST' on the LARC2 rear panel, then power on the LARC2.

NOTE: Do not touch any of the faders until the power on diagnostics test results have been checked. (Touching the faders will clear the power on diagnostics test results displayed on the Meter Bd. LED's).

NOTE: If any of the Red or Yellow LED's on the Meter Board remain lit, a diagnostic error has occurred.

NOTE: When the LARC2 has entered the Interactive Diagnostics menu mode, the Fader Touch and A/D converter information for the fader being touched and/or moved is displayed on the Meter Board LED's. The Red LED's (1-8) indicate which fader (1-8) is being touched respectively. The Yellow LED's act as a level meter which displays the value read from the A/D converter of the fader being touched and/or moved (1=Min, 8=Max). This is useful for quickly checking the operation of the Faders and A/D converters circuitry, but the Fader/Motor Test performs more accurate testing at higher resolution.

The 'Interactive Diagnostics' menu is displayed on the LCD display after approximately 8 seconds as shown in the example below:

```
Voltage raw 00000305, mvolts 11312
BootRom diag file built Apr 11 2000, 16:08:02
BootRom Version 0.13  App. version 247
For test:          Press:                 (or on the DeBug port, enter:)
  Self Test__________ 'PROGRAM' + 'REGISTER'.             ('s')
  LCD Test___________ 'PROGRAM' + 'STORE'.                ('c')
                         Press 'ENTER' to change pattern  ("Enter")
  Key Test___________ 'PROGRAM' + 'EDIT'.                 ('k')
  LED Test___________ 'PROGRAM' + 'CONTROL'.              ('e')
                         Press 'MACHINE' to advance.      ('n')
                         Press 'ENTER' to stop.           ("Enter")
  JoyStick Test______ 'PROGRAM' + 'JOYSTICK'...           ('j')
                         Move joystick completely around the edges TWICE.
                         (Hold 'CONTROL' to see data.)    ('c')
                         Press 'ENTER' to stop            ("Enter")
  Fader/Motor Test___ 'PROGRAM' + 'FINE ADJ'.             ('f')
  LEXICON Test_______ 'PROGRAM' + 'LEXICON'.              ('l')
  Memory Test________ 'PROGRAM' + 'MUTE ALL'.             ('m')
  Repetitive Test____ 'PROGRAM' + 'MACHINE'.              ('a')
                         Hold 'LEXICON' to quit           ("Enter")
  Diagnostics Suite___'PROGRAM' + 'BANK'.                 ('d')
To exit _____________ 'MUTE ALL' + 'MUTE MACH'.           ('R')
```

NOTE: The top line of the 'Interactive Diagnostics' menu displays the voltage test readings raw value and its conversion to millivolts, line 2 displays the date and time of the Boot ROM build, and line 3 displays the Boot ROM and Application version (the actual text may vary).

The Interactive Diagnostic tests are executed from the 'Interactive Diagnostics' menu by pressing two keys simultaneously. For example: pressing the 'PROGRAM' + 'REGISTER' keys would execute the 'Self Test'. The key combinations used to execute the Interactive Diagnostic tests are listed in the table below:

TEST NAME:	**KEY COMBINATION:**
Self Test	**PROGRAM + REGISTER**
LCD Test	**PROGRAM + STORE**
KEY Test	**PROGRAM + EDIT**
LED Test	**PROGRAM + CONTROL**
Joystick Test	**PROGRAM + JOYSTICK**
Fader/Motor Test	**PROGRAM + FINE ADJ**
LEXICON Test	**PROGRAM + LEXICON**
Memory Test	**PROGRAM + MUTE ALL**
Repetitive Test	**PROGRAM + MACHINE**
Diagnostics Suite	**PROGRAM + BANK**
To exit	**MUTE ALL + MUTE MACH**

IMPORTANT: Always follow the instructions which appear on the LARC2 LCD display or Debug Terminal when performing any of the Interactive Diagnostic tests.

Self Test:

NOTE: These are the same tests that are executed during the Power On Diagnostics.

Prior to the execution of the Power On Self Tests, the Realtime Clock is tested. This test verifies the operation of the 32.768kHz crystal on the SA-1100.

TEST 1: Motor Waveform Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 2: Motor Control Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 3: A/D Control Registers Test

This test writes to control registers in SA-1100, then verifies the value written can be read.

TEST 4: A/D Self Test

This test reads the MIN, MID and MAX values based on the reference voltage of the A/D converter.

TEST 5: (Not Used)

TEST 6: External PS/2 Keyboard Test

This test initializes the External Keyboard, and tests for the presence of a keyboard connected to the AUX port of the LARC2 by sending 8 characters out the port, and monitors any data that is received. The data received is then compared to what was sent.

NOTE: This test requires an External Keyboard connected to the 'AUX' port. Otherwise the test will fail when an External Keyboard is not present. Diagnostic error messages are also sent to the Debug Port to indicate when a failure has occurred as shown in the example below.

****ERR**KB01** TXRDY= 0. should be 1, GPIO= fffc7ec**
****ERR**KB02** IBFULL= 1 should be 0, Stat= 12, GPIO= fffc7ec**
****ERR**KB03** Keyboard Timeout**

TEST 7: Host Port (Loop Back) Test

This test checks for the presence of a Loop Back Plug connected to the HOST port of the LARC2 by sending 8 characters out the port, and monitors any data that is received. The data received is then compared to what was sent.

NOTE: This test requires a Female RS-422 Wraparound Plug installed in the 'HOST' port. Otherwise the test will fail when the Loop Back Plug is not present. A diagnostic error message is also sent to the Debug Port to indicate when a failure has occurred as shown in the example below:

Loop Back Not installed

TEST 8: Keystuck & Fader Touch Test

This test checks for stuck keys on the Main Board, or if any of the Faders were being touched during the Power On Diagnostic tests.

LCD Test:

This test is used to verify the operation of LCD display circuitry by displaying various attributes of the LCD display, which includes a display of vertical color bars, dimming the LCD display, turning the LCD display off and on, and displaying a white screen with a red border. When the test is executed, the 'ENTER' key is used to advance (step) through six different screens to verify the operation of the LCD display, as described in the table below:

STEP:	DESCRIPTION:
1	The LCD displays vertical color bars at full brightness
2	The LCD displays Vertical Color Bars that are dimmed
3	The LCD display is turned off
4	The LCD displays Vertical Color Bars that are dimmed
5	The LCD displays Vertical Color Bars at full brightness
6	The LCD displays a white screen with a red border

NOTE: The white screen with a red border (from Step 6 above) is the best screen to use for verifying there are no defective pixels (which would appear as black dots) on the LCD display. This is also useful for checking the alignment of the LCD display with the Display Housing assembly.

Key Test:

This test is used to verify the operation of the Fader Touch circuitry for each of the (8) faders, and the (45) keys on the Main Board keypad. When the test is executed, the (8) faders are tested first, followed by the (45) keys. During the test, the names of the keys pressed are sent to the LCD display, and also to the Debug Port.

NOTE: Pressing the 'Lexicon' key will exit the test. Be sure the 'Lexicon' key is the last key pressed when testing the keys. The 'Lexicon' key can also be used to bypass the Fader Touch tests if necessary.

NOTE: If a fader is touched when the test is executed an error message is sent to the LCD display, and also to the Debug Port as shown in the example below:

A fader is being touched.
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

NOTE: If the Key Test is exited prior to testing all of the keys, an error message is sent to the LCD display, and also to the Debug Port reporting the names of keys that were not pressed. An example of the error message displayed when the 'JOYSTICK' and 'FINE ADJ' were not pressed is shown below:

Failure on key JOYSTICK
Failure on key FINE ADJUST
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

LED Test:

This test is used to verify the operation of the LED's and driver circuitry of the (12) Main Board LED's, and the (24) Meter Board LED's. When the test is executed, the 'MACHINE' key is used to advance the test to the next LED.

IMPORTANT: When the LARC2 is reset, all of the LED's on the Main Board and Meter Board are turned on, and the brightness of the LED's may vary considerably because the LED's are not being scanned. The LED Test should always be used whenever it is necessary to compare the brightness of the LED's because the LED's are being scanned during the LED Test.

When the test is executed, the following message is sent to the LCD display, and also to the Debug Port as shown in the example below:

Press 'MACHINE' ('n' on debug port) to advance, 'ENTER' when finished.

NOTE: When the LED Test is exited before all of the LED's have been tested, an error message is sent to the LCD display, and also to the Debug Port as shown in the example below:

Did not check every LED.
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

Refer to the table below for more information about the behavior of the Main Board 'keypad' and Meter Board LED's during the LED Test:

LOCATION:	STEP #: LED: (X=ON)	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
MAIN BD	MUTE MACH		X														X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MAIN BD	MUTE ALL			X																																					
MAIN BD	MACHINE				X								X																												
MAIN BD	ENTER					X								X																											
MAIN BD	CONTROL						X																																		
MAIN BD	STORE							X																																	
MAIN BD	REGISTER								X																																
MAIN BD	PROGRAM									X																															
MAIN BD	BANK										X																														
MAIN BD	EDIT											X																													
MAIN BD	JOYSTICK														X																										
MAIN BD	FINE ADJ															X																									
METER BD	#1 GREEN	X		X	X	X	X	X	X	X	X	X	X	X	X	X	X																								
METER BD	#2 GREEN	X																X																							
METER BD	#3 GREEN	X																	X																						
METER BD	#4 GREEN	X																		X																					
METER BD	#5 GREEN	X																			X																				
METER BD	#6 GREEN	X																				X																			
METER BD	#7 GREEN	X																					X																		
METER BD	#8 GREEN	X																						X																	
METER BD	#8 YELLOW	X																							X																
METER BD	#7 YELLOW	X																								X															
METER BD	#6 YELLOW	X																									X														
METER BD	#5 YELLOW	X																										X													
METER BD	#4 YELLOW	X																											X												
METER BD	#3 YELLOW	X																												X											
METER BD	#2 YELLOW	X																													X										
METER BD	#1 YELLOW	X																														X									
METER BD	#1 RED	X																															X								
METER BD	#2 RED	X																																X							
METER BD	#3 RED	X																																	X						
METER BD	#4 RED	X																																		X					
METER BD	#5 RED	X																																			X				
METER BD	#6 RED	X																																				X			
METER BD	#7 RED	X																																					X		
METER BD	#8 RED	X																																						X	

Joystick Test:

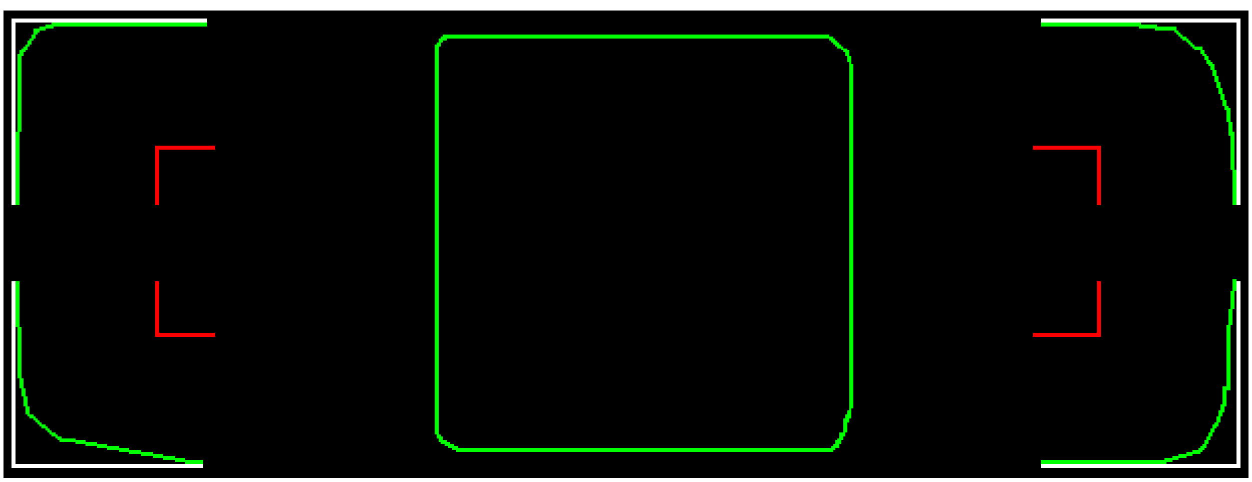
This test is used to verify the operation of the Joystick hardware and circuitry. This test has been designed to display the movement of the Joystick on the LCD display. During the test, the Joystick must be moved along the outside edges (farthest from the center) a minimum of two times.

When the test is executed, the following screen will appear on the LCD display:



The outer (White) brackets in the corners of the LCD display represent the lower limits of the Joystick Test. The inner (Red) brackets on the LCD display represent the upper limits of the Joystick Test.

During the test, an image (box) is drawn in the center of the LCD display as the Joystick is moved, which represent the values read from Joystick A/D converter. The image displayed in each corner of the LCD display represents a magnified view of the four corners from the image drawn in the center of the LCD display (as shown in the example below).



NOTE: The image drawn in the center of the LCD display should always be drawn in the same direction as the joystick (up/down & left/right) movement. This test is useful for verifying the correct wiring of the Joystick.

NOTE: During the test, the Meter Board RED and GRN LED's act as a level meter which displays the values read (X/Y position) from the joysticks A/D converter (1=Min, 8=Max) for troubleshooting purposes.

The RED LED's indicate the Left/Right position of the joystick, and the GRN LED's indicate the UP/DOWN position of the joystick.

When a failure has occurred, an error message is sent to the LCD display, and also to the Debug Port as shown in the example below:

**** Test invalid. Did not test edges enough. ****
**** Joystick touched inner boundary. ****
(Be careful not to move joystick away from the edges after beginning test.)
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

NOTE: During the test, there is a special mode that is available for debugging purposes which sends the values read (X/Y position) from the joysticks A/D converter to the LCD display when the 'CONTROL' key is pressed as shown in the example below.

Horzntl 1023 , Vertical 118

Fader/Motor Test:

is test has been designed to verify the ability of the Fader and Motor circuitry to detect the current position of the fader, then move the fader in the proper direction until it has reached the next pre-designated position. When the test is executed, all of the (8) faders are moved to their minimum position, and are moved slowly to their maximum position, then back down to their minimum position. During the test, the A/D converter values of the (8) Faders are monitored to determine their respective positions.

When a failure has occurred, an error message is sent to the LCD display, and also to the Debug Port as shown in the example below:

***** FAIL *** Timeout on fader 2.**
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

Lexicon Test:

This test is used to verify the operation of the piezo transducer circuitry. This test has been designed to read the values from the piezo transducer's A/D converter, and verify that two (Max) values can be achieved. When the test is executed, the 'Lexicon' key is pressed & released until a Max value below 300, and a Max value above 600 is displayed on the LCD display.

When a failure has occurred, an error message is sent to the LCD display, and also to the Debug Port as shown in the example below:

Did not hit full range.
****** Press '+' (or Enter on debug port) key to acknowledge.**

Press the '+' key on the LARC2, or press 'ENTER' on the Debug Terminal to continue.

Memory Test:

This test performs a non-destructive memory test on all memory locations of the DRAM above the memory locations where the Boot ROM was copied (from C0008000h to C8000000h). The test first writes 55555555 (hex) into these memory locations of the DRAM, then the same memory locations are read to verify the data written in these locations is correct. This write/read sequence is also performed using the (hex) values FFFFFFFF and a Walking 1's pattern. Refer to the table below for the hex to binary conversion of the data patterns:

HEX VALUE:	MSB BINARY CONVERSION: LSB
55555555	0101 0101 0101 0101 0101 0101 0101 0101
FFFFFFFF	1111 1111 1111 1111 1111 1111 1111 1111
1	0000 0000 0000 0000 0000 0000 0000 0001
2	0000 0000 0000 0000 0000 0000 0000 0010
4	0000 0000 0000 0000 0000 0000 0000 0100
8	0000 0000 0000 0000 0000 0000 0000 1000
10	0000 0000 0000 0000 0000 0000 0001 0000
20	0000 0000 0000 0000 0000 0000 0010 0000
40	0000 0000 0000 0000 0000 0000 0100 0000
80	0000 0000 0000 0000 0000 0000 1000 0000
100	0000 0000 0000 0000 0000 0001 0000 0000
200	0000 0000 0000 0000 0000 0010 0000 0000
400	0000 0000 0000 0000 0000 0100 0000 0000
800	0000 0000 0000 0000 0000 1000 0000 0000
1000	0000 0000 0000 0000 0001 0000 0000 0000
2000	0000 0000 0000 0000 0010 0000 0000 0000
4000	0000 0000 0000 0000 0100 0000 0000 0000
8000	0000 0000 0000 0000 1000 0000 0000 0000
10000	0000 0000 0000 0001 0000 0000 0000 0000
20000	0000 0000 0000 0010 0000 0000 0000 0000
40000	0000 0000 0000 0100 0000 0000 0000 0000
80000	0000 0000 0000 1000 0000 0000 0000 0000
100000	0000 0000 0001 0000 0000 0000 0000 0000
200000	0000 0000 0010 0000 0000 0000 0000 0000
400000	0000 0000 0100 0000 0000 0000 0000 0000
800000	0000 0000 1000 0000 0000 0000 0000 0000
1000000	0000 0001 0000 0000 0000 0000 0000 0000
2000000	0000 0010 0000 0000 0000 0000 0000 0000
4000000	0000 0100 0000 0000 0000 0000 0000 0000
8000000	0000 1000 0000 0000 0000 0000 0000 0000
10000000	0001 0000 0000 0000 0000 0000 0000 0000
20000000	0010 0000 0000 0000 0000 0000 0000 0000
40000000	0100 0000 0000 0000 0000 0000 0000 0000
80000000	1000 0000 0000 0000 0000 0000 0000 0000

When a Memory Test failure is encountered, the test will stop and loop continuously at the failed address location. The address where the error occurred, along with the data sent, and the data received is sent to the LCD display and also to the Debug Port.

NOTE: The Memory Test will run for approximately 2 minutes. The LARC2 will return to the 'Interactive Diagnostics' menu when the Memory Test is complete.

Repetitive Test:

This test was designed to exercise the LARC2 hardware during the Burn In cycle of the Manufacturing Test process. Refer to the following instructions for the execution of the Repetitive Test.

- Press & hold down the 'PROGRAM' + 'ENTER' keys while powering on the LARC2 by connecting the barrel end of the external power supply cord to the connector labeled 'POWER' on the LARC2 rear panel.

- Release the 'PROGRAM' + 'ENTER' keys when the chase pattern appears on the Meter Board and Keypad LED's.

NOTE: When the 'PROGRAM' + 'ENTER' keys are used to enter the Interactive Diagnostics, the #8 RED LED will be lit to indicate that a keystuck error has occurred. This is because the 'PROGRAM' + 'ENTER' keys were being held during the Power On Diagnostic Tests. This behavior is normal, and is not a fault with the LARC2.

Press the 'PROGRAM' + 'MACHINE' keys simultaneously to execute the 'Repetitive Test'.

NOTE: During the 'Repetitive Test' the Meter Board and Keypad LED's are lit sequentially (one LED at a time). The following diagnostic tests are executed in the sequence shown in the table below:

TEST:	DESCRIPTION:
LCD Display	*Eight different screens are displayed on the LCD Display*
Fader/Motor Test	*The same test that is used during Interactive Diagnostics*
Memory Test	*The same test that is used during Interactive Diagnostics*

Diagnostics Suite:

This Diagnostic Suite was designed to help reduce the test time during the Manufacturing Test process by automatically executing all of the Interactive Diagnostics one test after the other in the order listed below:

1. **Self Test**
2. **LCD Test**
3. **KEY Test**
4. **LED Test**
5. **Joystick Test**
6. **Fader/Motor Test**
7. **Lexicon Test**
8. **Memory Test**

OPTION BOARD Menu:

The following selections are available from the 'Option Board Menu' mode when the LARC2 Option Board is installed in the LARC2, and is connected to a debug terminal as shown below:

```
*       LARC2 Menu file built Apr 11 2000, 14:52:36     *
* Bootrom Version 0.13
************************************************************


 1]   Display Register                        X]   Download via XModem
 2]   Set Register                            F]   Flash Operations
 3]   Dump Memory                             K]   Keyboard Echo
 4]   Set Memory                              D]   Interactive Diagnostics
 5]   Erase FLASH                             I]   Enable Interrupts
 7]   Display Ethernet Information            L]   Loop on read
 8]   Set Up Ethernet Information             S]   Diagnostics Suite
 9]   Download Image Via Ethernet(ESHELL)     Z]   ZModem Download
 A]   Load from PCMCIA Flash                  O]   Option-Board Test
 B]   Boot @ d0000000
 C]   Fill Memory with a Pattern


>>
```

NOTE: The top line of the 'Interactive Diagnostics' menu displays the date and time of the Boot ROM build, and line 2 displays the Boot ROM version (the actual text may vary).

Descriptions for the most commonly used selections available from the Option Board Menu are as follows:

9] Download Image Via Ethernet(ESHELL):

This menu selection is used to download the LARC2 Program Flash image (larc2_enet.bin) via a PCMCIA Ethernet card in order to reduce test time during the manufacturing test process.

B] Boot @ d0000000:

This menu selection is used to Boot the LARC2 application software from the Option Board Menu. The following options are available: Boot from Ram (the image downloaded to DRAM), Boot from PCMCIA, Boot from Flash (Program Flash), Decompress from Flash, as shown in the menu below:

```
************************************************
*       App Boot Options
************************************************
r] Boot From Ram
p] Boot from PCMCIA
f] Boot from Flash
d] Decompress from Flash
X] Download via Xmodem:
```

This menu selection is used to download the LARC2 Boot ROM (boot.rom) and/or Program Flash image (larc2.rom) via the Debug Port on the LARC2 Option Board using the Xmodem transfer protocol.

F] Flash Operations:

This menu selection is used for programming the Program Flash memory with the LARC2 application (Program App) and/or to program the Boot ROM (Burn Boot Flash). These options are available from the menu shown below:

```
************************************************
*       Flash Management Options
************************************************
w] Program App
b] Burn BOOT flash
e] Erase PROGRAM flash
s] Save a copy of the BOOTROM
r] Restore BOOTROM
2] Program STAGE2
```

D] Interactive Diagnostics:

This menu selection is used to enter the Interactive Diagnostics Menu from the Option Board Menu.

S] Diagnostics Suite:

This is the same test that resides on the Interactive Diagnostics Menu. This menu selection can also be used to execute the Diagnostics Suite from the Option Board Menu.

Z] ZModem Download:

This menu selection is used to download the LARC2 Boot ROM (boot.rom) and/or Program Flash image (larc2.rom) via the Debug Port on the LARC2 Option Board using the Zmodem transfer protocol.

O] Option-Board Test:

This menu selection is used to execute the Option Board Test from the Option Board Menu.

NOTE: The remaining selections available from the Option Board Menu were designed specifically for use during the LARC2 hardware development, and are outside the scope of this document.

MISCELLANEOUS TESTS:

Option Board Test:

The Option Board Test was designed for debugging problems encountered when programming the Program Flash memory by verifying the operation of the PCMCIA interface. This test resides in the Option Board Menu, and requires the LARC2 Option Board (with 32MB PCMCIA Flash Memory card) installed in the Option Board Connector on the LARC2. The Option Board Test can only be executed from a Debug Terminal connected to the Debug port of the LARC2 Option Board.

When executed, the test checks for the presence of the PCMCIA Flash Memory card first by checking the card type. If there is no PCMCIA Flash Memory card installed, it reports that fact and will not run any further. Then it checks the header of the PCMCIA Card for the existence of a legitimate 960L application, and warns if a header is present, with the option to quit or continue (destroying the cards contents). It also checks the size of the card, so that it will not attempt to test memory that isn't present. Then it performs the following tests as shown in the example below.

NOTE: In the example below, the information sent to the Debug port was captured using a Debug Terminal. The comments added below describe the operations that are performed during the test:

Checking Card Type
Card Type 1
Testing PCCard flash memory of size 0x2000000 (33554432 decimal)
Erasing Flash PCcard...(This takes a few moments.)
Erasing block 0

This portion of the test erases the PCMCIA Flash Memory card.

Erasing block 1
Erasing block 2
Erasing block 4
Erasing block 8
Erasing block 16
Erasing block 32
Erasing block 64
Erasing block 128

This portion of the test verifies the address lines on the PCMCIA Flash Memory card are functioning properly by writing a walking 1's pattern across the address lines. During the test, the current address values are written to memory, then the same memory locations are read to verify the data written in these locations is correct. If any errors are detected the failure results are reported, and the test then waits for acknowledgement of the error. NOTE: The first address bit is not tested because the test is writing 16-bit values.

Writing to 0x3c000000
Writing to 0x3c000002
Writing to 0x3c000004
Writing to 0x3c000008
Writing to 0x3c000010
Writing to 0x3c000020
Writing to 0x3c000040
Writing to 0x3c000080
Writing to 0x3c000100
Writing to 0x3c000200
Writing to 0x3c000400
Writing to 0x3c000800
Writing to 0x3c001000
Writing to 0x3c002000
Writing to 0x3c004000
Writing to 0x3c008000
Writing to 0x3c010000
Writing to 0x3c020000
Writing to 0x3c040000
Writing to 0x3c080000
Writing to 0x3c100000
Writing to 0x3c200000
Writing to 0x3c400000
Writing to 0x3c800000
Reading from Flash PCcard...

This portion of the test reads each value and compares it to what was written. If any errors are detected the failure results are reported, and the test then waits for acknowledgement of the error.

Address 0x3c000000, GD 0x0000, BD 0x0000
Address 0x3c000002, GD 0x0001, BD 0x0001
Address 0x3c000004, GD 0x0002, BD 0x0002
Address 0x3c000008, GD 0x0003, BD 0x0003
Address 0x3c000010, GD 0x0004, BD 0x0004
Address 0x3c000020, GD 0x0005, BD 0x0005
Address 0x3c000040, GD 0x0006, BD 0x0006
Address 0x3c000080, GD 0x0007, BD 0x0007
Address 0x3c000100, GD 0x0008, BD 0x0008
Address 0x3c000200, GD 0x0009, BD 0x0009
Address 0x3c000400, GD 0x000a, BD 0x000a
Address 0x3c000800, GD 0x000b, BD 0x000b
Address 0x3c001000, GD 0x000c, BD 0x000c
Address 0x3c002000, GD 0x000d, BD 0x000d
Address 0x3c004000, GD 0x000e, BD 0x000e
Address 0x3c008000, GD 0x000f, BD 0x000f
Address 0x3c010000, GD 0x0010, BD 0x0010
Address 0x3c020000, GD 0x0011, BD 0x0011
Address 0x3c040000, GD 0x0012, BD 0x0012
Address 0x3c080000, GD 0x0013, BD 0x0013
Address 0x3c100000, GD 0x0014, BD 0x0014
Address 0x3c200000, GD 0x0015, BD 0x0015
Address 0x3c400000, GD 0x0016, BD 0x0016
Address 0x3c800000, GD 0x0017, BD 0x0017

This portion of the test verifies that all of the data lines on the PCMCIA Flash Memory card are functioning properly. The data lines are tested by writing/reading a walking 1's pattern into the first memory location.

Writing 0x0001 Reading 0x0001
Writing 0x0002 Reading 0x0002
Writing 0x0004 Reading 0x0004
Writing 0x0008 Reading 0x0008
Writing 0x0010 Reading 0x0010
Writing 0x0020 Reading 0x0020
Writing 0x0040 Reading 0x0040
Writing 0x0080 Reading 0x0080
Writing 0x0100 Reading 0x0100
Writing 0x0200 Reading 0x0200
Writing 0x0400 Reading 0x0400
Writing 0x0800 Reading 0x0800
Writing 0x1000 Reading 0x1000
Writing 0x2000 Reading 0x2000
Writing 0x4000 Reading 0x4000
Writing 0x8000 Reading 0x8000
All okay. Press Enter...

Program Flash Data Checking:

When the Program Flash memory is programmed (during the Program App routine), the data written to the Program Flash memory is verified by performing a byte by byte comparison of the data written to the Program Flash memory and the downloaded data that is currently in the DRAM memory.

In the event that a failure has occurred, the data sent, data received, and failed address information is displayed as shown in the example below:

Ok, be patient...
Programming block 28.0
Checking data...
**** Error. GD 6e617645, BD 6e617607, address 08180000**

The location of the failure(s) can be found by converting the hexidecimal values to their binary equivalent. The example below shows that the data sent (GD) does not match the data received (BD) at bits 1 and 6.

GD 6e617645 = 110 1110 0110 0001 0111 0110 0100 0101

BD 6e617607 = 110 1110 0110 0001 0111 0110 0000 0111

Address 08180000 = 1000 0001 1000 0000 0000 0000 0000

NOTE: The data checking that is performed during the Program App routine when the Program Flash memory is programmed only verifies the data that was written to the flash, and does not test the unused portion of the flash memory.

Chapter 7 Theory of Operation

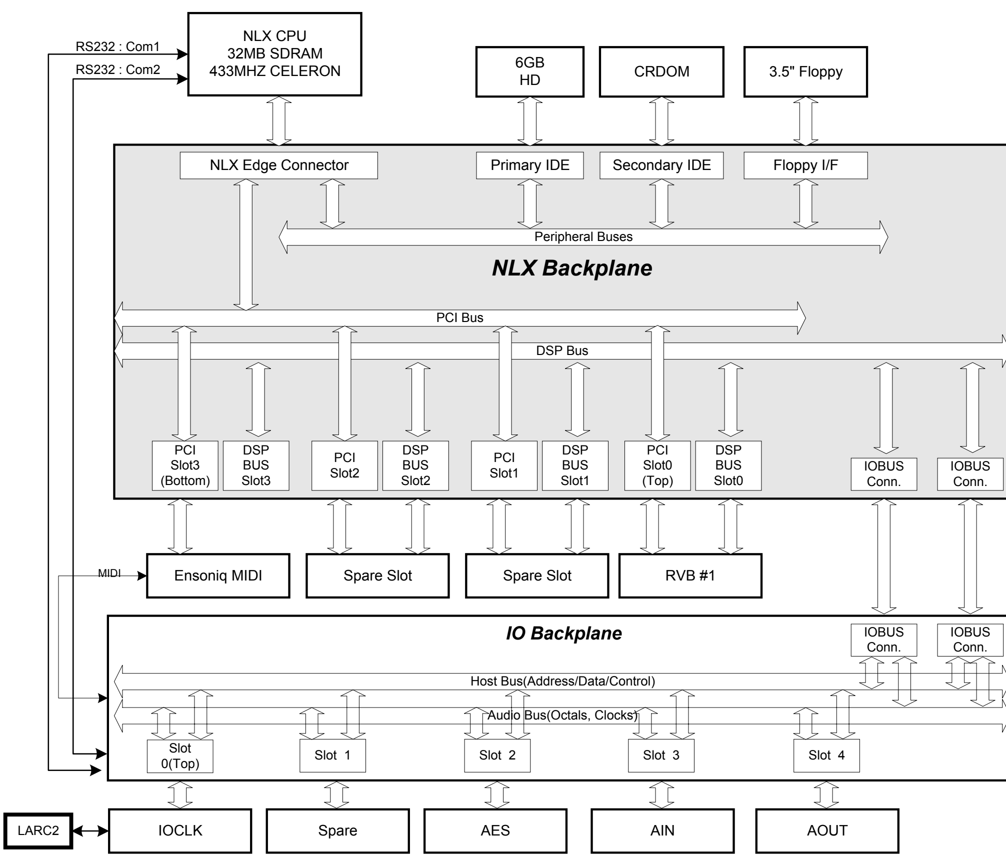
NLX Backplane

This section describes the theory of operation of the 960L IO Backplane card.

Overview

The NLX PC form factor is an industry standard platform originally developed by Intel. The significant difference between this form factor and other commodity PC form factors is that all system interconnect is removed from the motherboard and located on a separate riser card. Since there are no cables connected to the motherboard, it can be easily removed. The NLX backplane is a custom NLX riser card that Lexicon developed to meet the needs of the integrated PC and its peripherals along with providing Lexicon specific functionality not possible utilizing other standard PC form factors.

The 960L NLX backplane provides the interconnect between the PC motherboard, DSP cards on the PCI bus, IDE hard drive, IDE CDROM drive, Floppy drive, IO backplane, and power distribution and management functions. Communication between DSP cards and the IO cards in the system are provided over a Lexicon proprietary control and audio interface using a second set of PCI style connectors. The following system block diagram highlights its place within the 960L system.



System Block Diagram

Circuit Description

This section is a page by page description of the 960L NLX Backplane card schematic.

NLX Interface (Sheet1)

J6 is a standard NLX riser card connector. This interface contains the signal interconnect for the following functions:

- PCI Bus (The 960L support up to 4 PCI slots)
- ISA Bus (not supported by 960L)
- Primary (Hard Drive) and Secondary IDE (CDROM) Interfaces
- Floppy Interface
- Power, supply, management and control

PCI Interface (Sheets 2, 3, 4)

Sheet 3 contains the series termination resistors for various PCI signals. This sheet also contains the pullups for the slot specific signals (e.g. GNT/, REQ/, IRT/, …).

Sheet 4 and 5 are the PCI slot connectors. The 960L support the 5V PCI, v2.2, standard. Slot addressing and identification are accomplished through standard PCI bus algorithms. In PCI parlance, Slot 0(IDSEL0) is the topmost PCI slot in the 960L and Slot 3(IDSEL3) is the bottommost slot. This is significant in that not all NLX motherboards support four (4) PCI slots. From a mechanical standpoint (i.e. least mechanical keep out constraints), the top slots are the most valuable in that the PCB in these slots can support more surface area (i.e. more real estate = more functionality per slot) and the least significant slots (i.e. Slot 0, 1, …) are supported first by NLX motherboards. For a detailed understanding, please refer to the PCI Specifications, V2.2.

IO Connectors (Sheet 5)

Sheet 5 contains the ISA interface (J5), primary (J9) and secondary (J8) IDE and floppy drive(J7) interface connectors. The ISA bus connector is not populated, as the current NLX motherboard no longer supports ISA. By convention, the primary IDE interface is connected to the hard drive and the secondary interface is connected to the CDROM drive. The 960L, 3.5", HD, floppy drive is connected to the floppy drive connector, J7.

The actual hardware that supports all of these interfaces resides on the NLX motherboard itself.

Miscellaneous Connectors (Sheet 6)

Much of the circuitry on this page is not populated. It was originally included for experimental or future use. This includes components: J18, J16, U2, U1, J17, J25, J19, J23, J24, and the resistors and capacitors associated with them.

The only functionality which is in use are power on and reset circuits. J20 connects the front panel standby/power switch and LED to the NLX backplane. This switch is a momentary type which signals the NLX motherboard to either turn on or turn of the power by pulsing the SOFT_ON_OFF/ control signal. The NLX motherboard lights the power on LED accordingly.

A standard PC hard reset signal is provided. A momentary switch on the inside of the 960L chassis behind the front panel connects to the NLX backplane via J21.

IOBUS & Power Connectors (Sheet 7)

The NLX backplane and the IO backplanes are connected by two 40-pin ribbon cables, which connect to J14 and J15. This interface is comprised of an 8-bit, non-multiplexed address and data system control bus and serial audio data and clock signals. The cards in the IO backplane can also interrupt the DSP cards by asserting the IOBUS_INT/ signal. The ALL_MUTE/ signal is provided to allow for a hardware assisted system wide mute.

The power provided by the NLX power supply comes in on connector, J26. This is an NLX standard connector and pinout. The power connectors provide, +/-5x, +3.3v, +/-12v, and +5VSB supply rails. NLX supplies can be remotely controlled. The NLX motherboard is capable of shutting off the power supply by

asserting the PS_ON/ signal. It does so on system software shutdown or when the STANDBY/POWER switch is pressed.

DSPBUS Connectors (Sheet 8, 9)

Communication between DSP cards and the IO cards in the system are provided over a Lexicon proprietary control and audio interface using a second set of PCI style connectors, J10-J13.

Passive termination networks (R015/R109/R110, R104/R107/R108, R106/R111/R112) are used on TMIX_CKI, TMIX_CKI/2, TMIX_WCKI to maintain signal integrity (i.e. manage signal reflections and levels).

All serial audio data signals, TMIX1_SERD* and TMIX2_SERD* are pulled up by resistors, R13-R20, 127-R140. The capacitors on these pages are for power supply decoupling and bypassing.

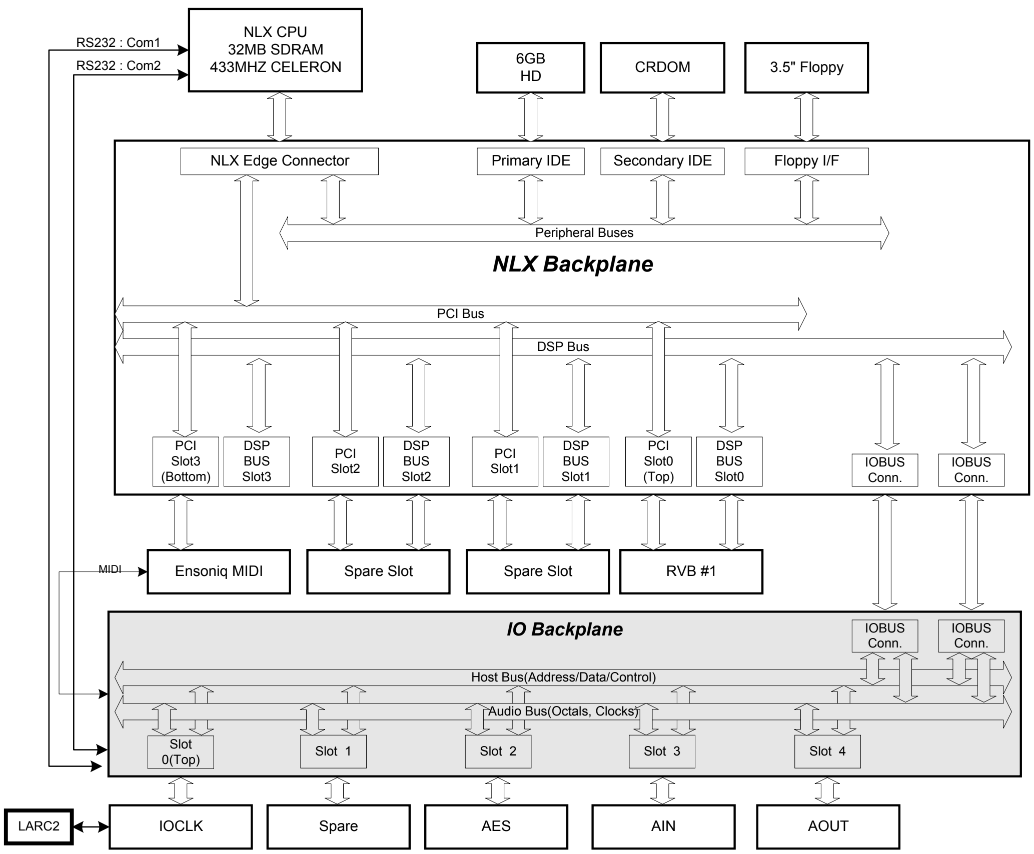
I/O Backplane

Introduction

This section describes the theory of operation of the 960L IO Backplane card.

Overview

The 960L IO Backplane provides the interconnect between the DSP cards located on the NLX Backplane and the system clock and control, and audio IO cards which comprise a 960L effects system. It also connects, via ribbon cables, the PC motherboard RS232 serial and MIDI ports to the IOCLK PCB. The following system block diagram highlights its place within the 960L system.



System Block Diagram

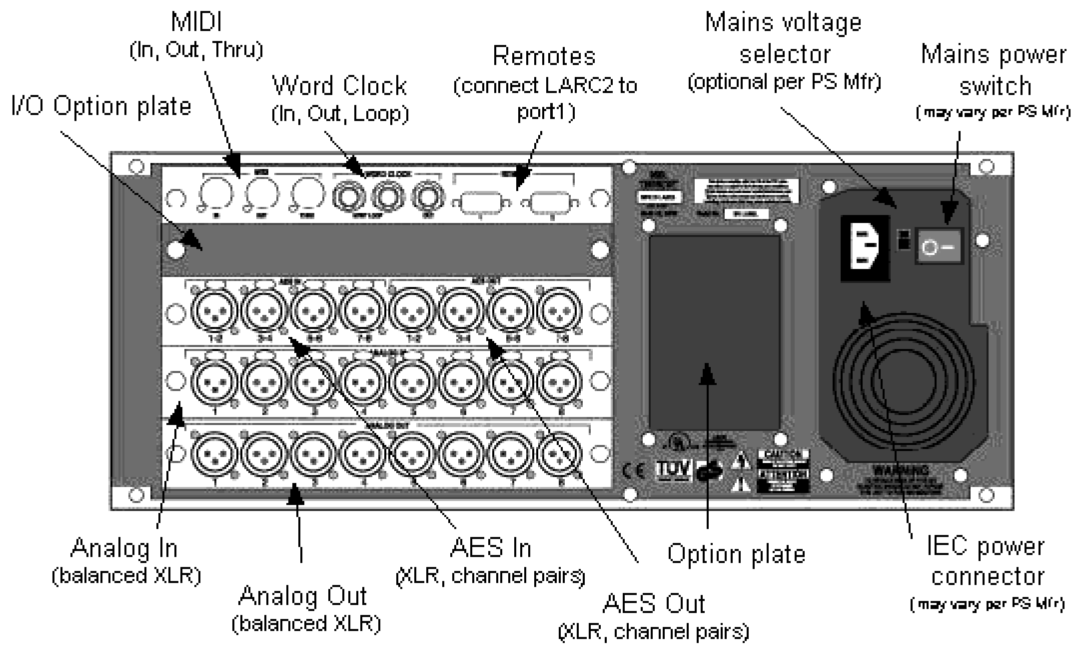


Figure 1-1 960L Rear Panel

The IO Backplane supports five, uniquely addressable card slots, which are accessed from the rear of the 960L chassis (Fig 1-1). With the exception of the slot address decodes, the interface signals to each slot is identical. However, because of mechanical and specific electrical constraints, not all cards can or should be randomly located. The recommended slot ordering is:

Slot 1(top)	IO Clock PCB
Slot 2	Spare Slot
Slot 3	AES PCB
Slot 4	AIN PCB
Slot 5(bottom)	AOUT PCB

Table 1-1 Recommended Rear Panel Slot Ordering

The most critically placed PCB is the IO Clock card. This card supplies the master bit (TMIX_CKI) and word clock (TMIX_WCKI) for the entire system and needs to be located in the topmost slot to drive one end of the TMIX_CKI transmission line. (Note: 256FS, 128FS, 64FS, and FS clocks are also available but are not currently used by any IO card.)

Circuit Description

This section is a page by page description of the 960L IO Backplane card schematic.

Sheet 1

NLX to IO Backplane Connectors (Sheet 1)

The NLX backplane and the IO backplanes are connected by two 40-pin ribbon cables which connect to J10 and J11. This interface is comprised of an 8-bit, non-multiplexed address and data system control bus

and serial audio data and clock signals. R15, R16, and C1 provide filtering for the SYSTEM_RESET/ signal provided by the DSP cards. The cards in the IO backplane can also interrupt the DSP cards by asserting the IOBUS_INT/ signal. The ALL_MUTE/ signal is provided to allow for a hardware assisted system wide mute. Pullup resistors, R28-R32 are provided to establish a default undriven signal level for signals PWR_OK, IOBUS_INT/, IOBUS_DS/, IOBUS_AS/, ALL_MUTE/, respectively.

IO Backplane Slot Connectors

The IO backplane bus is comprised of the system control bus, serial audio clocks, serial audio data (in octal format), MIDI pass thru connections, RS232 pass thru connections. Each IO card plugs into 96-pin EURO style connectors, J1-J5.

TMIX1_SERD(3:0)	1:0/AIN, 3:2/DIN	O	Pullup
TMIX1_SERD(11:10)	Expansion	O	Pullup
TMIX2_SERD(3:0)	5:4/AOUT/7:6(DOUT)	I	Pullup
TMIX2_SERD(11:8)	Expansion	I	Pullup
TMIX_WCKI	TMIX "512fs" clk	O	Active
TMIX_CKI/2	TMIX 256fs clock	O	Active
TMIX_CKI	TMIX "wc" clk	O	Active
WCLK	Master WCLK	O	Active
256FS	Master 256FS	O	Active
128FS	Master 128FS	O	Active
64FS	Master 64FS	O	Active
SLOT_WCLK	System WC	3st	Active
SLOT_SEL/	One unique sel. per slot	I	
IOBP_ADDR(8:0)	Control Bus Addr	I	
IOBP_DATA(7:0)	Control Bus Data	IO	
RESET/	Master Reset	I	Pullup
Preview_WCK INT/	Preview Word Clock INT	3st	Active
IOBP_RD/	Control Bus Read	I	On IOBP
IOBP_WR/	Control Bus Write	I	On IOBP
IOBP_AS/	Control Bus AS	I	On IOBP
PWROK	Power OK	I	Pulldn
ALL_MUTE/	Panic Mute	OD/OC	Pullup
IOBP_DS/	XCVR EN	I	On IOBP
IOBP_INT/	Interrupt	OD/OC	Pullup
+12V	From NLX Supply	I	
+5V	From NLX Supply	I	
-12V	From NLX Backplane	I	
GROUND	From NLX Supply	I	
MIDI_TX	From NLX IO Panel	I	
MIDI_RX	From NLX IO Panel	O	
RS232 TX1	From NLX IO Panel	I	
RS232 TX2	From NLX IO Panel	I	
RS232 RX1	From NLX IO Panel	O	
RS232 RX2	From NLX IO Panel	O	

Table 2-1 IO Backplane Signal List

Slot Addressing

Decoder, U1, provide slot addressability by decoding the system control bus address signals ADDR11:9. Each slot is allocated a 512 byte address space. The address map is as follows:

Slot 1(top)	0x000-0x1FF
Slot 2	0x200-0x3FF
Slot 3	0x400-0x5FF
Slot 4	0x600-0x7FF
Slot 5(bottom)	0x800-0x9FF

Table 2-1 Slot Address Map

At startup, the system software polls each slot to detect the presence of an IO card. When no card is present in a slot, a default DATA bus value of 0xFF is provided by pullup resistors, R11-R14, and R24-R28 to signify this condition.

Clock Terminations

Passive termination networks (R40/R41/R45, R38/R39/R44, R36/R37/R43, R33/R34/R42, R2/R3/R1) are used on the local clock signals (IOBUS_256FS, IOBUS_128FS, IOBUS_64FS, and IOBUS_FS to manage signal reflections and levels. Currently, none of these local FS related clocks are used by any IO card.

Sheet 2

Power

Power is provided to the IO card in two ways. The +5v, +12v rails come directly from the 960L power supply via connector, J9. The –12v rail is supplied by the NLX backplane via connectors J11 (sheet 1).

MIDI

The MIDI interface signals come from a MIDI card located on the NLX backplane. Signals are carried over a 15 pin ribbon cable to connector, J8.

RS232

The two RS232 ports on the PC motherboard are connected to the IO backplane using 10-pin ribbon cables. COM Port 1 connects connector J6 and COM Port 2 connects to connector J7.

Miscellaneous

The serial audio data signals, TMIX1_SERD* and TMIX2_SERD* are pulled up by resistors, R4-R10, R17-R23. Capacitors, C2, C11 are bypass capacitors.

I/O Clock card - Input/Output and Clock Generator card

The I/O Clock card provides external interfaces and clock generation for the digital audio subsystems. Interfaces for midi control and external wordclock sync are supported, along with ports for the LARC2 remote control for the 960L. Clocks can be derived from internal crystal timebases or from external sources via an on-board Phase-Locked Loop (PLL). The supported sampling rates are 44.1 or 48kHz in single-speed mode or 88.2/96kHz in double-speed mode.

Midi Interface

On-board signal-conditioning circuitry interfaces external midi current-loop signals with internal logic levels, which connect to a midi adapter card located in slot 3 (bottom slot) of the NLX backplane. Midi input on J3 (MIDI INPUT) is current-limited by R18 and optically-coupled by U11 (HCPL0601), which converts it to 5V logic level MIDI_RXD (high=marking, low=spacing). Midi input is echoed directly, without decoding delay, to J5 (MIDI THRU) via inverter U12 and current-driver transistor Q2 (2N3904), with R23 and R24 providing current limiting. MIDI_RXD connects to the IO backplane, which in turn feeds it to the midi adapter, which contains the asynchronous serial receiver that interfaces the serial data to the NLX motherboard. Midi transmission originates on the midi adapter and arrives on the IO backplane as logic level MIDI_TXD (high=marking). Inverter U12 and transistor Q1 drive J4 (MIDI OUTPUT), with R20 and R21 providing current limiting.

Ttl Wordclock Interface

An external TTL-level wordclock-rate squarewave applied to BNC connector J6 (or J7) can be used as a reference for synchronizing the internal sample rate. The input automatically configures itself as either a 75-ohm termination or as a high-impedance bridging loop. Each connector contains an internally-switched 75-ohm terminating resistor which disconnects when an external mating BNC connector is present. With just one BNC cable connected, the resistor in the other connector terminates the line. With two BNC cables

connected, both resistors get disconnected and the input becomes a bridging, high-impedance loop, allowing the line to be chained to other equipment and terminated elsewhere in the system.

The input squarewave is applied to the high-impedance non-inverting input of line receiver U13 (75ALS180), that produces the buffered waveform BNC_WCIN. The receiver threshold is set at about 1.6V by resistors R25 and R26. BNC_WCIN is fed to a multiplexer implemented within the programmed logic of CPLD U2 (XC9572), where it can be selected by software to be the reference for the on-board PLL.

A squarewave derived from the internal wordclock, BNC_WCOUT, is generated by U2 and fed to the line driver section of U13. OUTPUT BNC J8 is driven by the non-inverting output of U13. Output impedance is around 15 ohms, and output voltage is typically 3.5Vpeak when loaded with 75 ohms to ground.

Larc2 Interface

J9 and J10, female 9-pin D-subminiature connectors, are ports for LARC2 remote control consoles, REMOTE 1 and 2. Each port delivers fused 12Vdc power and provides separate full-duplex RS-422 serial communication channels.

J9.5 delivers 12Vdc from the system 12V supply through self-resetting fuse PS1 (0.75Amp). Normally, the fuse exhibits a low series resistance, a few tenths of an ohm. When overloaded by currents >1.5Amp, the fuse undergoes self-heating and switches to a high resistance state due to the thermal characteristics of its material. This high resistance limits the current drawn from the supply under the overload condition. The fuse maintains the high-resistance state as long as it dissipates about 0.8W, or about 66mA at 12V, which is the short-circuit condition. The trip time is typically 0.2 seconds at 8 Amps, which is a severe overload. Smaller overloads can take many seconds to trip. Resetting occurs when the load is removed and the fuse cools, returning to the low-resistance state.

Full-duplex remote serial communication is based on RS-232 COM ports built into the NLX motherboard. U14 (75ALS180) forms the interface between the bipolar unbalanced RS-232 levels of the COM1 port and the unipolar balanced RS-422 levels of the REMOTE 1 port. The RS-232 signals from COM1 connect to the IO backplane J6 via a ribbon cable connected to the 9-pin D-sub connector on the IO panel of the motherboard. The backplane brings COM1 signals to J1 as RS232_TXD1/ and RS232_RXD1/ (marking=negative, spacing=positive). RS232_TXD1/ feeds the driver section of U14 through R27 and dual diode D9 (BAV99), which essentially limits the bipolar RS232 signal to a logic level TXD1/ within the range acceptable by U14. When the serial port is idle (i.e. marking), TXD1/ is low. The output of the U14 driver is wired to make TX1+ high and TX1- low, so the marking state of the differential RS422 signal is positive, according to convention. (The U14 driver is wired as an inverting stage because of the sense of RS232_TXD1/).

The receiver section of U14 accepts differential RS422 input from REMOTE 1 and produces logic-level signal RS232_RXD1/. As with the driver, the receiver is wired as an inverting stage, such that when the difference between RX1+ and RX1- is positive (i.e. marking), RS232_RXD1/ is low, in accordance with RS232 conventions. With no external connection to J9, R28 and R29 bias the differential pair in the marking (positive) state, overriding the default biasing of the receiver input. The RS232_RXD1/ logic level is fed directly to the COM1 RS232 line receiver on the motherboard. Although the line receiver normally expects wide-range bipolar RS232 levels, its input threshold is essentially TTL, and it operates properly when driven locally with conventional unipolar logic levels.

Similarly, REMOTE 2 communication is based on the COM2 RS232 port on the NLX motherboard. COM2 is implemented as a 10-pin header on the NLX motherboard, connected by ribbon cable to IO backplane J7.

CPLD Logic

U2 (Xilinx XC9572, sheet 2) is a Complex Programmable Logic Device, which is custom-programmed to perform several different functions. Unlike the FPGAs on other modules, the internal logic of the CPLD is permanently programmed, so no configuration needs to be loaded each time power is applied. The CPLD

forms most of the interface between the I/O backplane control, data, and clock buses and the on-board clock generating circuitry.

Pin	Name	Type	Description
Host Interfacse			
42	RESET/	INPUT	Not used.
33	ALL_MUTE/	OUTPUT	Not Used.
39	CS/	INPUT	CHIP SELECT/ - 0 : this slot is being selected, 1 : not selected
37	DS/	INPUT	DATA STROBE - data is captured on rising edge of DS/
35	WR/RD	INPUT	WR/RD - 0 : write operation, 1 : read operation
34	A0	INPUT	Address 0 - select which register is written/read to/from (see register description section)
7	D7	BIDIR	Data Bus <7> - data is written/read over this bus
8	D6	BIDIR	Data Bus <6> - data is written/read over this bus
9	D5	BIDIR	Data Bus <5> - data is written/read over this bus
11	D4	BIDIR	Data Bus <4> - data is written/read over this bus
12	D3	BIDIR	Data Bus <3> - data is written/read over this bus
13	D2	BIDIR	Data Bus <2> - data is written/read over this bus
14	D1	BIDIR	Data Bus <1> - data is written/read over this bus
18	D0	BIDIR	Data Bus <0> - data is written/read over this bus
Clocks			
28	BNC_WCLK	INPUT	External BNC wordclock input
40	SLOT_WCLK	INPUT	Wordclock from another slot on the IO backplane
25	PLL_512FS	INPUT	PLL master clock. The frequency of PLL_512FS is 512 times the TMIX_WCKI rate. Nominally 24.576 or 22.5792Mhz.
29	48K_512FS	INPUT	Local 24.576Mhz oscillator input
24	44K_512FS	INPUT	Local 22.5792 Mhz oscillator input
43	TMIX_CKI	OUTPUT	TMIX_CKI - TMIX master clock.
44	TMIX_CKI/2	OUTPUT	TMIX_CKI/2 – A clock that runs at half the rate of TMIX_CKI. All edge transitions are timed with the falling of of the TMIX_CKI clock.
1	TMIX_WCKI	INPUT	TMIX_WCKI - TMIX word clock. Rising edge denotes start of an octal frame. All edge transitions are timed with the falling of the TMIX_CKI clock.
2	B_256FS	OUTPUT	A clock signal whose frequency is 256 times the sample rate. All edge transitions are timed with the falling of the TMIX_CKI clock.
3	B_128FS	OUTPUT	A clock signal whose frequency is 128 times the sample rate. This signal is typically used as the I2S bit clock. The falling edge denotes the stqart of a bit cell. All edge transitions are timed with the falling of the TMIX_CKI clock.
4	B_64FS/	OUTPUT	A clock signal whose frequency is 64 times the sample rate. The falling edge denotes the start of the word clock period. All edge transitions are timed with the falling of the TMIX_CKI clock.
5	B_FS/	OUTPUT	A clock signal whose frequency is equal to the sample rate. All edge transitions are timed with the falling of the TMIX_CKI clock.
19	BNC_WCLK_OUT/	OUTPUT	A clock signal whose frequency is equal to the sample rate. This signal is identical to B_FS/, except when OSC_DRIVES_BNC is set in the CTLREG. All edge transitions are timed with the falling of the TMIX_CKI clock.
6	PVW_WCLK	OUTPUT	Preview word clock. This signal, when enabled via the PVWCLK_EN in the CTLREG, is driven by the BNC_WCLK or the SLOT_WCLK signal. The selection is determined by the state of the PVW_WCK_SEL field in the CTLREG.
PLL Signals			
22	PUMP_UP	OUTPUT	VCO pump up signal.
20	PUMP_DN/	OUTPUT	Active low, VCO pump down signal
26	LKERRDET	OUTPUT	PLL Lock error detected signal.
27	PLL_LOCKED	INPUT	Indicates that the PLL is locked to the selected word clock source. The state of this can be read from the CPLD CTLREG.

36	XTAL_EN	OUTPUT	Local oscillator output enable control. When negated, all oscillators are disabled to reduce signal noise created by the oscillators when not in use.
CPLD Support			
15,16, 17	TDI,TCK,TMS	INPUT	JTAG Interface. Not used except to program the part in place.
30	TDO	OUTPUT	JTAG Interface. Not used except to program the part in place.

Control Interface

The I/O Clock card appears as two, byte-wide ports on the I/O backplane databus IOBUS_DATA[7:0], at the addresses determined by the decoding of SLOT_SEL/ and one address bit, IOBUS_ADDR0. IOBUS_WR/RD determines the direction of data transfer (low=write, high=read), with IOBUS_DS/ being asserted low during data transfers. U2 captures write data on the rising edge of IOBUS_DS/.

IOBUS_RESET/ and PWROK are used to initialize various internal FPGA state. When low, ALL_MUTE/ forces the octal audio data lines(TMIX1_SERD0,1,2,3,10,11) to zero.

Register Descriptions

OFFSET ADDR	NAME	Access	Default Value	*Description*
0x00	**IDREG(7:0)**	**RO**	0x00	***Board ID***
	IDREG(7:4)	**RO**	0	**Type**(0=IOCLK PCB)
	IDREG(3:0)	**RO**	1	***Interface revision***
0x01	**CTLREG(7:0)**			
	CTLREG(7)	**RW**	0	**OSC_DRIVES_BNC**. Active High. When set, the BNC Output is derived from local 48K oscillator.(For test purposes only) The purpose is to loop the BNC OUT to the BNC IN and attempt to lock to it. This confirms that the BNC input and output paths circuits are functional
	CTLREG(6)	**RW**	0	**SEL_1X_CLKMODE**. Active Low. Set to zero for 44.1/48K, else one for 88.2/96k
	CTLREG(5:4)	**RW**	0	**WCKSEL(1:0)** - System Word Clock Source Select WCKSEL(1:0) = 0 Selects 48/96 Khz internal oscillator as word clock source WCKSEL(1:0) = 1 Selects 44.1/88.2Khz internal oscillator as word clock source WCKSEL(1:0) = 2 Selects EXT BNC signal as word clock source WCKSEL(1:0) = 3 Selects IO Backplane SLOT_WCK as word clock source
	CTLREG(3)	**RW**	0	***Preview Word Clock Select*** PVW_WCK_SEL = 0 Selects EXT BNC clock as this board's preview word clock source PVW_WCK_SEL = 1 Selects the current SLOT_WCK as this board's preview word clock source
	CTLREG(2)	**RW**	0	**PWCLK_EN** - Active High. Preview word clock enable. When asserted this board's selected preview word clock will be asserted onto the PREVIEW_WCLK pin on the IO Backplane. Care must be taken so that no more than one PCB on the IO backplane asserts it preview workclock onto the backplane.
	CTLREG(1)	**RW**	1	**XTAL_EN**. Active High. Enables XTAL Oscillators. This must be asserted to use osc's as internal clock source.
	CTLREG(0)	**W**	0	**TESTMODE**. Active High. For development purposes only. When enabled, OSC's drive system clock tree directly, bypassing the PLL.

Clock Bus Interface

All digital audio clocking in the 960L system is derived from U2 and associated on-board circuitry. Clocks from U2 are buffered by U1 (74FCTT244 or 74ABT244) and driven onto the I/O backplane, which distributes them to other modules.

All system clocks are derived from the PLL_512FS clock signal. The frequency of PLL_512FS is 512 times the rate fo TMIX_WCKI. The table below lists the rates of each system clock as a function of the system sample rate.

Signal	*Sample Rate*			
	44.1 Khz	**48 Khz**	**88.1 Khz**	**96 Khz**
PLL_512FS	*22.5792 Mhz*	*24.576 MHz*	*22.5792 Mhz*	*24.576 MHz*
TMIX_CKI	*22.5792 Mhz*	*24.576 MHz*	*22.5792 Mhz*	*24.576 MHz*
TMIX_WCKI	*44.1 Khz*	***48 Khz***	*44.1 Khz*	*48 Khz*
B_256FS	11.2896 Mhz	12.288 Mhz	22.5792 Mhz	24.576 MHz
B_64FS/	2.8224 Mhz	3.072 Mhz	5.6384 Mhz	6.144 Mhz
B_FS/	44.1 Khz	48 Khz	88.1 Khz	96 Khz
BNC_WCOUT	44.1 Khz	48 Khz	88.1 Khz	96 Khz

The external BNC wordclock can be used to derive system clocking. The 960L system software can first preview the incoming BNC wordclock by assigning it to the IO backplane SLOT_PCLK_INT/ signal. Once satified, the 960L system software can select the BNC word clock as the source for system clocking. Clock selection and preview clock enable are controlled by the control register, CTLREG in the U1 FPGA.

Clock Selection

Clocks can be derived from both on- and off-board frequency references.

The on-board references are two high-accuracy (10ppm) crystal oscillator modules U3 (24.576MHz) and U4 (22.5792MHz), that are connected to inputs of U2. These crystal frequencies are multiples of the standard 48/96kHz and 44.1/88.2kHz sampling rates, respectively.

Off-board references are sample-rate wordclocks that come either from the on-board BNC receiver circuitry described above, or from pin C5 of the I/O backplane. Other I/O modules can supply this wordclock via the backplane, so that a variety of external sources can provide the reference clock for the system, according to the specific type of I/O interface module.

PLL Support

Logic within U2 that is involved with the operation of the PLL is described below.

Phase-Locked Loop

All clocks that are distributed to the digital audio systems in the 960L ultimately derive from the oscillator in the on-board PLL (sheet 3). The PLL consists of a Voltage-Controlled Oscillator (VCO, U10, MC12148), a Phase/Frequency Detector (PFD) implemented within CPLD U2, and an active filter formed by op-amp U6 and associated circuitry. The VCO oscillates around the 22-24MHz range, depending on sample rate. The PFD and other logic within U2 lock the oscillator appropriately to whatever source is chosen to be the frequency reference. Reference sources affect the system only indirectly, when they become the reference for the PLL. Logic within U2 divides the VCO frequency to form the several system clocks that are distributed to the backplane. This clock tree, along with the action of the VCO, ensures continuous coherent clocking within the system.

The PFD operates at the single-speed wordclock rate in both single- and double-speed modes, i.e 48kHz at both 48 and 96kHz. The VCO frequency is always divided by 512 to form one input to the PFD. The other PFD input is derived from the chosen reference source, conditioned by other logic within U2 to be at the single-speed wordclock rate.

For internal crystal operation, a multiplexer within U2 selects the input from one crystal and divides it by 512 to become 48kHz or 44.1kHz, for U3 or U4, respectively. External wordclock sources (BNC, e.g.) get

divided by two, if necessary, to form single-speed wordclock from double-speed input. A final multiplexer chooses the reference source to be applied to the PFD logic. When neither crystal oscillator is in use, they both get disabled under software control by bringing XTAL_EN low. Multiplexing and other configuration of the logic within U2 is established according to the value written to the internal control register by software.

PLL Detailed Description

To ensure a high degree of VCO stability and constant loop gain, 5Vdc for the PLL (5VA) is supplied by a dedicated regulator, U7 (78L05), regulated from 12V. Diodes D5,D6 prevent large differences from existing between the 5V supplies. Within the PLL, 5VA is decoupled at multiple points with ferrites and bypass capacitors.

Phase-Frequency Detector

The PFD implemented within CPLD U2 is a well-known edge-detector type which compares the phase and frequency of two logic signals and detects zero error at zero phase. Here the PFD inputs are the selected reference wordclock and the single-speed wordclock derived from the VCO, both of which exist internal to the CPLD. If the VCO frequency is too low or too high, the PFD drives output pins of the CPLD with a train of mutually exclusive PUMP_UP or PUMP_DOWN/ pulses, respectively. As the VCO frequency changes to approach lock, one train of pulses of varying width is generated. When the frequencies are essentially equal, the pulses depend on the phase error between the two wordclock-rate signals. If the wordclock from the VCO lags the reference, due to approach from a lower frequency, PUMP_UP is generated, and PUMP_DOWN/ remains inactive. The opposite is true when approaching from a higher frequency. In an ideal PFD of this type, when the edges of the two wordclock waveforms within the CPLD are exactly in phase, neither pulse would occur; the zero-error phase-lock condition occurs when the edges are coincident. In the basic PFD, if the reference signal drops to zero frequency (i.e., is absent), the logic would assert PUMP_DOWN/ constantly, to try to force the VCO frequency to zero to match the reference. To prevent this, special logic in the PFD defeats PUMP_DOWN/ if the reference is lost, preventing the forced rapid drop of VCO frequency. Pulses from the CPLD are buffered by inverting stage U8 and become the UP/ and DOWN pulses fed to the active loop filter. U8 is supplied by the regulated 5V to clamp the pulses to a constant amplitude, removing any fluctuations that may be present on the main logic supply.

Voltage Controlled Oscillator

VCO U10 oscillates at a frequency which depends on L1 (1 uH), C35 (10pF), and the capacitance of varactor diode D7 (BB132). The output of U10 is around 700 mVp-p at a dc level of nearly 4V. This small signal is amplified and buffered by U9 (74HCU04) to develop PLL_512FS, a suitable logic level to drive CPLD U2. The oscillation frequency is normally in the range of 22 to 25MHz, and when in lock, oscillation is at an exact multiple (256 or 512) of the reference wordclock frequency.

The capacitance of D7 varies with its reverse-bias voltage; D7 is the element that allows voltage to control frequency. The anode of D7 is constant at about 1.7 V, established by the VREF pin of U10. The voltage at the cathode of D7 controls the VCO frequency. A greater positive voltage increases the reverse bias, reducing the capacitance and producing a higher VCO frequency. The network formed by R13, C24, FB8, and C37 helps keep high-frequency noise from being introduced at the cathode of D7, to reduce undesirable modulation of the VCO.

The range of oscillation for the VCO is from around 18 to 30 MHz, and control voltage is typically 4 to 6 volts when locked to 44.1 to 48kHz wordclocks (22.579 to 24.576 MHz).

Active Filter

Op-amp U6 (NJM4580) and associated circuitry form an integrator that serves as the active loop filter. The non-inverting input of U6 is biased at 2.5V by R7 and R8, and bypassed to ground by C22. The feedback capacitors C20 and C23 integrate the current introduced to the summing node by input resistors R9 and R11. R9 connects to logic level UP/ through series diode D3, and R11 connects to DOWN through series diode D4.

PLL Action

PLL action can be understood by first disregarding the effect of R10 and D2 in the active filter. In a perfect lock condition, neither the UP/ or DOWN logic level is asserted, so there is ideally no summing-node current because D3 and D4 are both reverse-biased, and therefore the voltage out of integrator U6 holds at some constant value. The VCO output is correspondingly constant, and its frequency and phase are exactly the constant value required to satisfy the PFD lock condition. In lock, there are no error signals to integrate. The correct control voltage exists and remains constant, at a value that was attained by integrating errors that occurred previously.

If the PFD generates UP/ pulses, either because frequency is too low or because phase is lagging, the integrator output voltage rises in increments that depend on the width of the UP/ pulses. When UP/ is low, D3 is forward biased and current flows through R9, charging the integrator capacitors. As the voltage rises, so does the frequency, and eventually the feedback action of the loop reduces the low-frequency/lagging-phase error to zero. The loop is satisfied and no further phase error occurs, so no further change to the VCO output occurs, which is the locked condition described above. A similar description applies to approach from the opposite direction. The magnitude of the up and down current pulses is nominally the same due to the 2.5V bias at the non-inverting input of U6.

If the VCO voltage at the cathode of D7 drops below 1.7V, the varactor begins to forward bias, and the VCO may completely cease to oscillate. D2 in the feedback path of U6 limits the VCO voltage to a low value of about 1.8V to ensure that the VCO always oscillates. At normal VCO operating voltages, D2 is reverse-biased and has negligible effect.

Jitter

To a degree, a PLL locks to the average of the reference frequency, rejecting short-term variations in phase, or jitter. The ability of the loop to track or reject variations in the reference phase is characterized by its jitter gain as a function of jitter frequency. This PLL is a second-order system. Its jitter gain is slightly overdamped due to R12, with a corner frequency around 150Hz principally determined by C20 in conjunction with the dc gain around the loop.

The jitter gain of the PLL and the intrinsic jitter of the VCO both exceed the requirement of AES3-1992 Amendment-1-1997.

Phase Detector Offset

As a practical matter, it is undesirable to operate the PFD at zero phase error. Because finite response times are involved in the logic that generates the UP/ and DOWN error signals, the PFD has a zone around zero-phase where it is non-linear, which causes undesirable loop operation. Improved loop performance is achieved by intentionally introducing a small dc error in the integrator, by means of R10. A small current from the summing node to ground through R10 acts to raise the output voltage and VCO frequency. To maintain lock, the loop compensates for this by developing a narrow positive DOWN pulse whose integral over one period is equal and opposite to the effect of R10, such that there is no net dc into the summing node. R10 is chosen to require a compensating DOWN duty cycle of about 1/128, and this small phase error in the PFD keeps it away from the zero-phase point. In lock, then, the PLL wordclock applied to the PFD is made to lead the reference wordclock by a constant phase offset, 1/128 of the wordclock period, so the PLL wordclock is not aligned with the reference. Within the CPLD, an additional wordclock is produced that is delayed (lags) by precisely this amount. It is this wordclock, which is almost perfectly aligned with the reference that is distributed for use throughout the 960L. The PLL wordclock that actually feeds the PFD has no visibility outside the CPLD.

Lock Detector

If the clocks from the PLL are not closely aligned with the reference, the PLL is considered to be unlocked. If lock is not within plus or minus 1/128 of a wordclock period on any clock cycle, logic within the CPLD generates a LKERRDET pulse, which triggers integrating one-shot U5. R6 and C8 set the timing of U5 at about 50 msec. The output of U5 is returned to the CPLD where it can be polled by software to ensure the

quality of phaselock and proper operation of the audio systems in the 960L. If lock remains within tolerance and no LKERRDET pulse occurs for 50 msec, U5 times out and the system is considered to be in lock. During lock capture, U5 gets retriggered frequently, so PLL-LOCKED/ does not get asserted at all, and the software can tell that the PLL is not locked. On-board LED D1 is driven directly from U5 to give a visible indication of the UNLOCKED condition.

Default Operation

By default, the CPLD configures the PLL to lock internally to crystal U3, producing a 48kHz-sampling rate when power is first applied to the card.

Power Supply

Power conditioning for the I/O Clock card involves local filtering and regulation of supplies from the backplane.

Main 5VD from the backplane supplies the CPLD and other digital logic.

The 12V supplies from the backplane (+12VSUP/-12VSUP) are filtered by FB1/FB2 and associated capacitors to supply +/-12V to the PLL active filter op-amp. +12VSUP also supplies the REMOTE connectors through fuses as described previously.

Analog Input card

The Analog Input card consists of eight channels of A/D conversion and associated input circuitry (sheets 1-4), bus interface fpga and connector (sheets 5,6) and on-board power conditioning (sheet 7). This card is plugged into the IO backplane which is accessed from the rear of the 960L chassis. The following system block diagram highlights its place within the 960L system.

Overview.

The Analog Input card is based on the AK5393 delta-sigma A/D converter, which accepts 2 channels of analog input and produces a pair of 24-bit digital audio samples at nominal rates up to 96kHz. Four converters provide the 8 channels of A/D conversion. High impedance differential inputs accept balanced or unbalanced signals at +24dBu maximum level on XLR connectors. Additional circuitry supplies the conditioning necessary to drive the differential 5Vp-p A/D input. The design supports nominal sample rates of 44.1/48kHz in single-speed mode and 88.2/96kHz in double-speed mode.

The following detailed circuit description applies to channel 1 (sheet 1). The seven other channels are similar.

Input Buffer

Signals at pins 2 and 3 of input XLR connector J2 are ac-coupled by C83 and C85 and attenuated by voltage dividers R130/ R129 and R132/R131, respectively. Differential input impedance is >50kohms, common mode impedance is >13kohm, and low-frequency response is <0.1dB down at 1Hz. Voltage division by 2 (-6dB) reduces a +24dBu level on either XLR pin to a maximum of +18dBu (8.7Vpeak) at the inputs of unity-gain buffers U20. The series resistances of R130, R132 prevent damage from excessive current if the input is overdriven. The common-mode component out of U20 is sensed by U16, which scales it by approximately -0.66. The output of U20 is also applied to the summing network formed by R49, 50,51 and 52, which scales it by approximately 0.4 and subtracts the common-mode component scaled by approximately 0.6 x .66=0.4. The common-mode voltage is substantially removed, and only the differential-mode component of the input signal appears at the input of unity-gain buffer U8, regardless of whether the applied input is balanced or unbalanced. The dc voltage at the non-inverting input of U16 is set at 2.5Vdc by R97,98 to create the offset that biases the A/D converter in the middle of its 5V range. Due to the gain of the stage, the dc level at the output of U16 is (1+0.66) x 2.5V=4.15V, which then is scaled back down by the summing network and appears at 2.5V at the inputs of U8. R81 supplies part of the dc current drawn by the summing network, reducing the dc load on U16. With +24dBu balanced input, the voltage out of each side of U20 is +/- 4.35Vpeak, the two sides have opposite phase, and there is no ac signal developed at the output of U16. The resulting fullscale differential signal at U8 is 7Vp-p. If the input is single-ended, the driven side of U20 develops +/- 8.7Vpeak, and U16 output swings between about 1.3 and 7 volts to balance the differential input to U8, which is still 7Vp-p.

U8 drives the differential A/D converter input through a low-impedance attenuating RC filter network consisting of R33, R26, R34, and C36. The network scales 7Vp-p signals down to 4.9Vp-p to match the nominal fullscale input level of the converter, so digital fullscale corresponds to +24dBu at the input connector. The single-pole 180kHz lowpass filter attenuates energy at the 128FS A/D sampling frequencies by >55dB, while passband response is flat within 0.2dB to 40kHz.

Common Mode Performance

Good common-mode rejection requires well-matched gains at the two input buffers and on boths sides of the summing/balancing network, where unequal common-mode gain on the two signal paths can convert a common-mode signal to an apparent differential-mode signal. Precision 0.1% resistors are used as appropriate to ensure that the minimum common-mode rejection ratio of the input circuitry is better than -45dB. Other resistors affect differential gain, but not common-mode rejection, and 1% precision is sufficient.

With a full-scale signal, the allowable additional input common-mode voltage range is at least +18dBu (+/-8.7Vpeak), limited by the clipping level of U20. Unwanted hum and noise at the input are unlikely to reach such high levels, but for a single-ended input, half the signal is common mode at this level.

A/D Converter

A/D converter U4 (AK5393) is powered on its VD pin by the main 5VD system power from the backplane, and on its VA pin by higher-quality 5VA regulated on-board by U3. Power is decoupled by ferrites FB3, FB4 and bypassed by C10, 11,12,13.

The channel 1 analog input is applied to the left stereo input AINL. The associated internally-developed reference voltages VREFL and VCOML are filtered by C37, 51,27.

U4 operates its serial digital audio port in I2S mode, SMODE[2:1]=1,0. U4 receives I2S framing and bitclock ADLRCK/ and ADSCK12/ from interface fpga U1 (sheet 4) and delivers two channels of 24-bit serial digital audio back into U1. AD12_SDO carries channel 1 and 2 data as left and right, respectively. Master clocks to the four A/D chips are distributed on separate lines from one pin of U1. MCK12 connects to U4, the converter for channels 1 and 2. Two A/D logic inputs are under the control of host software, via the U1 interface. CONV_RESET/ and DFS0 are applied to all four A/D chips in parallel. DFS1, connected to the TEST pins, is grounded by 0-ohm jumper R1.

Signal Polarity

There are no inversions in the analog signal path, so a positive voltage between J2.2 and J2.3 appears as a positive differential signal between AINL+ and AINL- and produces a positive digital value fed into the system via interface U1.

System Interface Logic

Fpga U1 (Xilinx XCS05, sheet 5) is the interface between the I/O backplane control, data(host and audio), and clock buses and the A/D converters and their associated controls. When power is applied to the card, the FPGA automatically receives its internal configuration from companion SROM U2. Configuration takes a few tens of msec, after which the onboard logic assumes its default state and is ready to be interrogated/programmed by system software.

Control Interface

The Analog Input card appears as two, byte-wide ports on the I/O backplane databus IOBUS_DATA[7:0], at the addresses determined by the decoding of SLOT_SEL/ and one address bit, IOBUS_ADDR0. IOBUS_WR/RD determines the direction of data transfer (low=write, high=read), with IOBUS_DS/ being asserted low during data transfers. U1 captures write data on the rising edge of IOBUS_DS/. Two pins of the FPGA are control outputs whose states get programmed from the host computer. CONV_RESET/ and DFS0 control all the A/D converters in parallel. DFS1 is permanently grounded as described above. IOBUS_RESET/ and PWROK are used to initialize various internal FPGA state. When low, ALL_MUTE/ forces the octal audio data lines(TMIX1_SERD0,1,2,3,10,11) to zero.

Register Descriptions

OFFSET ADDR	NAME	Access	Default Value	Description
0x00	**IDREG(7:0)**	**RO**	0x11	Board ID register
	IDREG(7:4)	**RO**	1	Type(1=AIN)
	IDREG(3:0)	**RO**	1	Interface revision number
0x01	**CTLREG(7:0)**			
	CTLREG(7:6)	**RW**	0X3	TMIX1 output serial octal drive select. 00 Drives TMIX1_SERD0/TMIX1_SERD1 octal pair 01 Drives TMIX1_SERD2/TMIX1_SERD3 octal pair 10 Drives TMIX1_SERD10/TMIX1_SERD11 octal pair 11 AIN Octals are not driven(all drivers are tristated)
	CTLREG(5)	**RW**	0	AKM5394EN : This enables the DFS1 driver for use with the AKM5394.

			Should only be set if the AKM5394 is used.
CTLREG(4)	**RW**	NA	Reserved
CTLREG(3)	**RW**	0	DFS1 : AKM5394 DFS1 control signal. Setting is only significant if AKM5394 AD is used.
CTLREG(2)	**RW**	0	DFS0. Double Speed Sampling Enable for AKM4393.
CTLREG(1)	**RW**	0	CONV_RESET. Active High. AD converter reset control line. All converters are reset when asserted. Software must assert, then negate CTLREG(1) to complete a soft reset sequence.
CTLREG(0)	**RW**	NA	Reserved

Clock Interface

The following onboard digital audio clocks are derived from bus clocks TMIX_CKI and TMIX_WCKI: I2S_FS/, I2S_64FS/, and I2S_256FS The bus clocks TMIX_CKI/2, IOBUS_WCLK/, IOBUS_64FS/, and IOBUS_256FS are not used. I2S_FS/ and I2S_64FS/ scale with sample rate FS. I2S_256FS is the master clock to the D/A converters, and is zzzcheck this (make sure 2x operation is right – see AOUT design) 256FS in single-speed mode and 128FS in double-speed mode. Source resistors in the clock lines reduce ringing due to reflections to provide proper clocking.

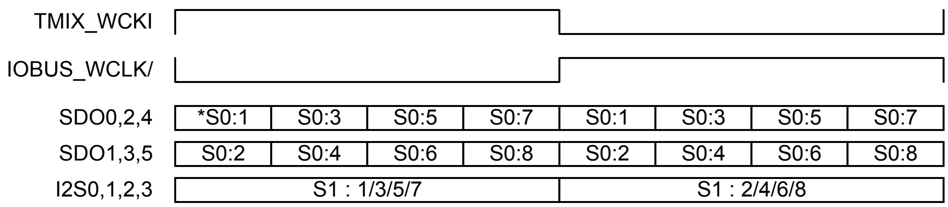
Digital Audio Interface

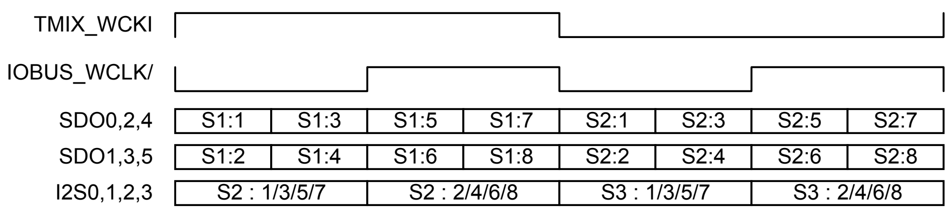
Audio data flows between the IO cards(e.g. Analog Input, Analog Output, AES) on the IO backplane and TMIX chips located on DSP(e.g. reverb) cards on the NLX backplane, over high speed serial audio channels called octals. TMIX chips define the octal format and timing. The bit rate of an octal is either 11.2896 Mbps for a 44.1Khz word clock or 12.288 Mbps for a 48Khz-word clock. An octal channel contains eight time slots. Each time slot can carry a 24-bit sample with up to 8 bits of status per sample. Note that the TMIX interface does not directly support double speed sampling rates.

Within U1, the four I2S stereo streams from the converters are merged into a pair of octal serial digital audio channels (at 11.2896 or 12.288 Mbps) to feed A/D input into the system via the I/O backplane.
At double-speed sampling rates(88.2/96Khz), each octal carries 4 audio samples during each I2S word clock period, so a pair can carry all 8 samples. Within a pair, samples from odd-numbered input channels (lefts) are split off and carried by one member of the pair(TMIX1_SERD0/2/10), even-numbered ones (rights) by the other(TMIX1_SERD1/3/11).

This division is the same at single-speed rates, and so is the bit rate, but fewer actual input samples are being provided by the converters. After a group of 4 samples has been clocked out at high speed, the next word clock has not occurred and there are not yet any new samples to follow. In this case, the FPGA hardware repeats the previous group, so that in single-speed mode, there are two successive groups of 4 samples within each word clock period that are the same. In both single- and double-speed modes, two high-speed channels are necessary to carry 8 samples.

U1 is capable of driving one of 3 alternate channel pairs, SDO0/1, SDO2/3, or SDO10/11, on the backplane. System software loads the CTLREG register within U1 to enable the drivers for one of the available pairs, driving 8 channels from one Analog Input card into the system.





channel number

Pin Descriptions

Pin	Name	Type	Description
Host Interface			
40	PWROK	INPUT	POWER OK - 0 : resets various internal state, 1: normal operation
44	RESET/	INPUT	RESET/ - 0 : resets various internal state, 1: normal operation
82	ALL_MUTE/	INPUT	ALL MUTE - 0 : forces SDI0-5 to zero, 1 : normal operation
50	CS/	INPUT	CHIP SELECT/ - 0 : this slot is being selected, 1 : not selected
47	DS/	INPUT	DATA STROBE - data is captured on rising edge of DS/
48	WR/RD	INPUT	WR/RD - 0 : write operation, 1 : read operation
66	A0	INPUT	Address 0 - select which register is written/read to/from (see register description section)
65	A1	INPUT	Not used.
62	A2	INPUT	Not used.
61	A3	INPUT	Not used.
60	A4	INPUT	Not used.
59	A5	INPUT	Not used.
58	A6	INPUT	Not used.
56	A7	INPUT	Not used.
67	D7	BIDIR	Data Bus <7> - data is written/read over this bus
68	D6	BIDIR	Data Bus <6> - data is written/read over this bus
69	D5	BIDIR	Data Bus <5> - data is written/read over this bus
70	D4	BIDIR	Data Bus <4> - data is written/read over this bus
72	D3	BIDIR	Data Bus <3> - data is written/read over this bus
77	D2	BIDIR	Data Bus <2> - data is written/read over this bus
80	D1	BIDIR	Data Bus <1> - data is written/read over this bus
81	D0	BIDIR	Data Bus <0> - data is written/read over this bus

Clocks

13	TMIX_CKI	INPUT	TMIX_CKI - master TMIX clock. All local clocks(I2S_FS/, I2S_64FS/, I2S_256FS) are derived from this clock and TMIX_WCKI. Input frequency is nominally 24.576Mhz or 22.5792Mhz for 48/96Khz and 44.1/88.2 sample rates respectively.
78	TMIX_CKI/2	INPUT	TMIX_CKI/2 - not used
51	TMIX_WCKI	INPUT	TMIX_WCKI - TMIX word clock. Rising edge denotes start of octal frame. Input frequency is 44.1Khz or 48Khz.
7	IOBUS_WCLK/	INPUT	Not used
35	IOBUS_64FS/	INPUT	Not used
10	IOBUS_128FS	INPUT	Not used
57	IOBUS_256FS	INPUT	Not used
8	I2S_FS/	OUTPUT	AD Frame Sync - falling edge denotes start of frame. Locally generated.
37	I2S_64FS/	OUTPUT	AD bit clock - falling edge denotes start of bit period. Locally generated.
9	I2S_256FS	OUTPUT	AD MCLK signal. Locally generated.
Pin	**Name**	**Type**	Description
Serial Audio			
3	I2S0	INPUT	I2S audio data for channels 1-2
4	I2S1	INPUT	I2S audio data for channels 3-4
5	I2S2	INPUT	I2S audio data for channels 5-6
6	I2S3	INPUT	I2S audio data for channels 7-8
19	SDO0	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 0. Tristate control is determined by the octal select field in the AIN control register(see register description for details)
18	SDO1	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 1.Tristate control is determined by the octal select field in the AIN control register(see register description for details)
14	SDO2	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 2.Tristate control is determined by the octal select field in the AIN control register(see register description for details)
20	SDO3	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 3.Tristate control is determined by the octal select field in the AIN control register(see register description for details)
24	SDO4	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 10.Tristate control is determined by the octal select field in the AIN control register(see register description for details)
25	SDO5	OUTPUT, TRISTATE	TMIX Octal data. Drives TMIX1 Octal 11.Tristate control is determined by the octal select field in the AIN control register(see register description for details)
Audio Control			
27	CONV_RESET/	OUTPUT	CONVERTER RESET. 0 : resets AD conveters, 1 : normal operation
26,28	DFS1,DFS0	OUTPUT	DFS1-0 : determines AD sample rate(1x vs 2x). (See AIN control register description for details)
FPGA Support			
32	MODE	INPUT	MODE - Serial download interface mode signal. Nomimally zero for loading from external SPROM
55	PROG/	INPUT	FPGA Program. 0 : causes the FPGA to reload its program from the external SPROM.
73	CCLK	OUTPUT	CCLK . Serial PROM clock signal
53	DONE	OUTPUT	FPGA DONE - Asserted when FPGA program cycle has completed.
41	INIT/	OUTPUT	FPGA serial download initialization signal.
71	DIN	INPUT	FPGA configuration data from SPROM
15,16, 17	TDI,TCK,TMS	INPUT	JTAG Interface. Not used
75	TDO	OUTPUT	JTAG Interface. Not used

Power Supply

Power conditioning for the Analog Input card involves local filtering and regulation of supplies from the backplane.

The main 5VD from the backplane is used by the fpga and the digital sections of the A/D converters.

The 12V supplies from the backplane (+12VSUP/-12VSUP) are filtered by FB1/FB2 and associated capacitors to supply +/-12V to the analog op-amps. +12VSUP also supplies U3 through a string of 5 dropping diodes to provide regulated +5VA for the A/D converters, which consume 4*130=520mA maximum. Diodes D7,D8 prevent large differences from existing between the 5V pins of the converters. Dropping diodes in series with U3 reduces the operating voltage, resulting in cooler operation.

Analog Output card

The Analog Output card consists of eight channels of D/A conversion and output circuitry (sheets 1-4), bus interface fpga and connector (sheets 5,6) and on-board power conditioning (sheet 7). This card is plugged into the IO backplane, which is accessed from the rear of the 960L chassis. The following system block diagram highlights its place within the 960L system.

Overview

The basis for each channel of analog output is a single AD1853 sigma-delta D/A converter, which converts 24-bit serial digital audio at its I2S port to differential analog current. The AD1853 is a two-channel device, applicable to conventional stereo conversion, but as applied in this design, the two channels are combined to form a single channel in order to achieve improved overall performance. Within a single wordclock period, the digital data pattern presented for the left channel is the inverse of the data for the right channel, while the analog outputs are cross-connected. In this way, one differential current pair is formed which is the in-phase sum of currents resulting from two simultaneous conversions. The differential current is converted to a differential voltage by low-noise operational amplifier stages, which drive a differential-input two-pole active filter stage. The unbalanced output of the filter is ac-coupled to the DRV134 differential transformerless line driver, to deliver fullscale differential output at +24dBm to XLR connectors. A two-pole muting relay prevents uncontrolled transients from appearing on the output when power is applied or removed from active circuitry. The design supports nominal sample rates of 44.1/48kHz in single-speed mode and 88.2/96kHz in double-speed mode.

Circuit Description.

The following detailed circuit description applies to channel 1 (sheet 1). The seven other channels are similar.

D/A Converter

D/A converter U6 (AD1853) is powered on its DVDD pin by the main 5VD system power from the backplane, and on its AVDD pin by higher-quality 5VA regulated on-board by U3. Power is decoupled by ferrites FB5, FB13 and bypassed by C29, 30,45,71. U6 operates its serial digital audio port in I2S mode, IDPM[1:0]=01. I2S signals I2S1/1,DAC_BICK/, and DAC_LRCK/ are provided by interface fpga U1 (sheet 4). Master clocks to the eight D/A chips are distributed from U1 in pairs, MCK12 driving U6and U7 (channels 1 and 2 respectively). The remaining four D/A logic inputs are under the control of host software, via the U1 interface. DAC_RST/, DAMUTE, DEEMPH, and 96K_EN are applied to all eight D/A chips in parallel. The SPI control port is not utilized; CLATCH, CCLK, and CDATA are connected to 0V.
Analog reference current for U6 is set at about 1mA by R22, filtered by C46, C47. The differential output currents OUTL and OUTR are connected out-of-phase, as described above. The combined currents OUTL+ and OUTR- are fed to one summing node of dual op-amp U14 (OPA2134) through ferrite FB22, with their counterparts similarly fed to the other summing node. The non-inverting inputs of U14 are biased at about 2.7V by the FILTR pin of U6, which sets the dc compliance voltage into which the D/A current sources are designed to operate.

U14 acts as a current-to-voltage converter (I/V converter), producing a differential voltage from the combined differential D/A currents. Each current-output pin of U6 sinks a bias of 1mA, and delivers full-scale signal current of +/-0.75mA around that bias point (.25 to 1.75 mA). The output voltage at U14.1 is determined by feedback resistor R92 (6.49k) balancing the net current into the summing node. The full-scale ac signal voltage developed at U14.1 due to OUTL+ would be +/- (0.75mA*6.49k) = +/-4.9V; it becomes +/-9.8V when the equal contribution of OUTR- is added.

A separate dc feedback scheme is used to eliminate dc bias from the outputs of U14. The feedback loop is formed by R49, R48, Q3, Q4, R47, R51, and ancillary components. Q4 supplies bias currents into the summing nodes through R47 and R51, while Q3 senses the sum of the outputs of U14 through R49 and R88. The combination of Q3 and Q4 has high current gain, and Q3 requires a negligible base current (<1uA) when the loop is nulled. R48 supplies a bias which must be offset by the currents through R49, R88,

so equilibrium is achieved when U14 outputs are somewhat below the Vbe of Q3, although not quite 0. A slight positive equilibrium point is desirable to accomodate the asymmetrical tolerances of the +/-12V system supplies as well as the asymmetrical output capability of the OPA2134, with the objective of maximizing the voltage range available for the audio signal. In addition to compensating for D/A bias current, the dc feedback also compensates for the FILTR compliance voltage, which requires another 0.4mA through each bias resistor. The presence of R47 and R51 at the summing nodes increases the noise gain of the I/V converter stages, but the effect decreases as the resistance increases, so large values are used. Q4 derives the bias current from VB, which is about +30Vdc. R47 (and R51) develop a voltage of around 2.4mA*10k=24V, so the collector of Q4 operates at about 28V, filtered by C93. The bias voltage at this point is common mode, so any noise present is rejected to a high degree by the differential signal stages.

By eliminating dc bias in the output of the I/V converters, their usable range is available for developing a large audio signal, which is favorable for achieving a high signal-to-noise ratio. Full-scale ac signal voltage at U14.1 is 9.8Vpeak (19dBu).

The sigma-delta current from the D/A has substantial components at frequencies well above the audio band, and C121, C95, and C94 are important for accommodating and reducing this high-frequency content in the I/V conversion.

Filter

U22 and associated components form a 2-pole multiple-feedback active filter that further reduces the non-audio content of the analog output. This filter has a characteristic lying between Bessel and Butterworth, with a -3dB frequency around 120kHz. The overall filter characteristic of the channel is designed to have a flat frequency response well within 0.5dB out to 40kHz and to exhibit a transient response consistent with the enhanced temporal/spatial resolution available at the double-speed 88.2/96kHz sampling rates. Mid-band gain is around 0.45 (-6.9dB), producing a full-scale CH1 signal of about 18dBu (8.7Vpeak).

Output Driver

The output of the filter is ac-coupled by C157 to U26, a monolithic transformerless differential output line-driver (DRV134). The differential output is fed back via dc blocking capacitors C165,C166 to its sense inputs. The driver has an output impedance of 50ohms and a nominal voltage gain of 6dB when driving 600ohms. With this low output impedance, the output level with and without a 600ohm load (dBm vs. dBu) differs by <1dB. Full-scale output is nominally +24dBm, and the transformerless characteristic makes signal level insensitive to load imbalance (high common-mode output impedance). C181 placed directly across the 50-ohm differential output forms the final pole in the overall filter characteristic.

Power for U26, +/-VCC, is derived from capacitive charge pumps which augment the +/-12V system supplies to +/-18V nominal, unregulated (sheet 7, see below). The higher voltage accommodates a modest common-mode output voltage arising from some degree of load imbalance or an equivalent external source of output common-mode voltage, while providing the supply current necessary at program peaks. With a perfectly balanced load, each output leg referred to common is +18dBu full-scale, 8.7Vpeak, around 5-6V below clipping. The output can therefore tolerate up to several volts of peak common-mode voltage, regardless of how it arises.

Note that the output driver cannot produce full +24dBm level if the output is wired for single-ended unbalanced operation with one leg grounded, as this would result in a common-mode voltage of 18dBu, corresponding to a peak output voltage greater than 17V, beyond clipping level. If grounded unbalanced wiring is employed, the maximum digital signal that can be accommodated is around -2 dBFS.

Mute Relay

RY1 in the normally-closed position mutes the differential output by grounding pins 2 and 3 of XLR connector J2. When energized under software control, RY1 connects J2 to the active output circuitry.

Relays for each pair of channels are energized by one transistor when software sets RLY_MUTE/ to a high logic level.

Signal Polarity

A positive digital value entering interface U1 from the backplane is converted to the corresponding positive value in the right channel of the D/A I2S stream, and its binary complement in the left channel. This makes U14.1 positive (U14.7 negative), U22.7 (CH1) negative, and U26.3 (J2.2) positive, so a positive digital input value from the backplane produces a positive voltage on the conventional differential XLR output.

System Interface Logic

FPGA U1 (Xilinx XCS05, sheet 5) is the interface between the I/O backplane control, data (host and audio), and clock buses and the D/A converters and their associated controls. When power is applied to the card, the FPGA automatically receives its internal configuration from companion SROM U2. Configuration takes a few tens of msec, after which the onboard logic assumes its default state and is ready to be interrogated/programmed by system software.

Control Interface

The Analog Output card appears as two, byte-wide ports on the I/O backplane databus IOBUS_DATA[7:0], at the addresses determined by the decoding of SLOT_SEL/ and one address bit, IOBUS_ADDR[0]. IOBUS_WR/RD determines the direction of data transfer (low=write, high=read), with IOBUS_DS/ being asserted low during data transfers. U1 captures write data on the rising edge of IOBUS_DS/. Five pins of the fpga are control outputs whose states get programmed from the host computer. Four pins, DEEMPH, DAMUTE, DCA_RST/, 96K_EN, control all the D/A converters in parallel and the fifth, RLY_MUTE/, controls the mute relays, as already described. IOBUS_RESET/ and PWROK are not used. When low, ALL_MUTE/ forces zeroes on all I2S data lines, I2S0-7.

Register Descriptions

ADDR	NAME	Access	Default Value	Description
0x00	**IDREG(7:0)**	**RO**	0x21	Board ID register
	IDREG(7:4)	**RO**	2	Type(2=AOUT)
	IDREG(3:0)	**RO**	1	PCB Revision number
0x01	**CTLREG(7:0)**			
	CTLREG(7)	**RW**	NA	Reserved.
	CTLREG(6:5)	**RW**	0X3	Octal Select : selects which IOBUS octal pairs are rec'd by the AOUT FPGA 00 AOUT octals rec'd from TMIX2_SERD0/TMIX2_SERD1 01 AOUT octals rec'd from TMIX2_SERD8/TMIX2_SERD9 10 AOUT octals rec'd from TMIX2_SERD10/TMIX2_SERD11 11 AOUT input octals set to zero
	CTLREG(4)	**RW**	0	DEEMPHASIS. Active High. When asserted, hardware de-emphasis is enabled.
	CTLREG(3)	**RW**	0	RELAY_MUTE/. Active Low. When asserted. All D/A output relays are in the mute state
	CTLREG(2)	**RW**	0	DAC_RESET/. Active Low. When asserted, all DACs are in reset state. Software must assert, then negate CTLREG(2) to complete a soft reset sequence.
	CTLREG(1)	**RW**	0	DAMUTE. Active High. When asserted, DAMUTE enables the built in D/A soft mute capability. Refer to the AD1853 spec for details.
	CTLREG(0)	**RW**	0	96K_EN. Active high. When asserted, D/A's operate in double speed mode(88.2 or 96K)

Clock Interface

The following onboard digital audio clocks are derived from bus clocks TMIX_CKI and TMIX_WCKI: I2S_FS/, I2S_64FS/, and I2S_256FS The bus clocks TMIX_CKI/2, IOBUS_WCLK/, IOBUS_64FS/, and IOBUS_256FS are not used. Ancillary clocks for charge pumps are also derived from TMIX_CKI: VBOSCU/, VBOSCD, and VCCOSC (see below). I2S_FS/ and I2S_64FS/ scale with sample rate FS.

I2S_256FS is the master clock to the D/A converters, and is 256FS in single-speed mode and 128FS in double-speed mode. Source resistors in the clock lines reduce ringing due to reflections to provide proper clocking.

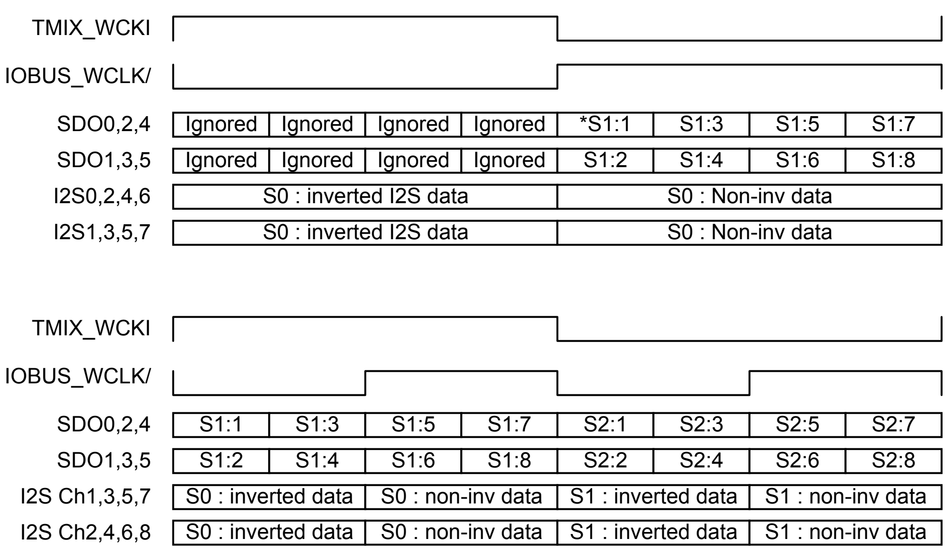
Digital Audio Interface

Audio data flows between the IO cards (e.g. Analog Input, Analog Output, AES) on the IO backplane and TMIX chips located on DSP (e.g. reverb) cards on the NLX backplane, over high speed serial audio channels called octals. TMIX chips define the octal format and timing. The bit rate of an octal is either 11.2896 Mbps for a 44.1Khz word clock or 12.288 Mbps for a 48Khz-word clock. An octal channel contains eight time slots. Each time slot can carry a 24 bit sample with up to 8 bits of status per sample. Note that the TMIX interface does not directly support double speed sampling rates.

Octal serial digital audio from the I/O backplane appears on 6 pins of U1 as 3 distinct pairs of channels. A controllable multiplexer implemented within interface U1 selects one pair of these octals to be the digital source for analog output. The octal pair selection is determined by the state of the octal select field in the CTLREG register within U1. Within U1, the selected 8 channels of high-speed data are converted to eight individual I2S streams, each carrying complement and true data as previously described, one for each D/A converter.

At double-speed sampling rates (88.2/96Khz), each high-speed channel can carry 4 audio samples during each word clock period, so a pair can carry all 8 samples. Within a pair, samples from odd-numbered input channels (lefts) are split off and carried by one member of the pair (SDO0/8/10), even-numbered ones (rights) by the other (SDO1/9/11).

This division is the same at single-speed rates, and so is the bit rate. However, only the last four octal time slots in each octal signal are used to derive the eight individual I2S audio streams. In both single- and double-speed modes, two high-speed octal channels are necessary to carry 8 samples.



channel number/data type

Pin Descriptions

Pin	Name	Type	Description
Host Interfacse			

40	PWROK	INPUT	POWER OK - not used
56	RESET/	INPUT	RESET/ - 0 : not used
82	ALL_MUTE/	INPUT	ALL MUTE - 0 : forces I2S data to zero(digital mute)
50	CS/	INPUT	CHIP SELECT/ - 0 : this slot is being selected, 1 : not selected
47	DS/	INPUT	DATA STROBE - data is captured on rising edge of DS/
48	WR/RD	INPUT	WR/RD - 0 : write operation, 1 : read operation
66	A0	INPUT	Address 0 - select which register is written/read to/from (see register description section)
65	A1	INPUT	Not used.
67	D7	BIDIR	Data Bus <7> - data is written/read over this bus
68	D6	BIDIR	Data Bus <6> - data is written/read over this bus
69	D5	BIDIR	Data Bus <5> - data is written/read over this bus
70	D4	BIDIR	Data Bus <4> - data is written/read over this bus
79	D3	BIDIR	Data Bus <3> - data is written/read over this bus
77	D2	BIDIR	Data Bus <2> - data is written/read over this bus
80	D1	BIDIR	Data Bus <1> - data is written/read over this bus
81	D0	BIDIR	Data Bus <0> - data is written/read over this bus
Clocks			
13	TMIX_CKI	INPUT	TMIX_CKI - master TMIX clock. All local clocks(I2S_FS/, I2S_64FS/, I2S_256FS) are derived from this clock and TMIX_WCKI. Input frequency is nominally 24.576Mhz or 22.5792Mhz for 48/96Khz and 44.1/88.2 sample rates respectively.
51	TMIX_CKI/2	INPUT	TMIX_CKI/2 - not used
78	TMIX_WCKI	INPUT	TMIX_WCKI - TMIX word clock. Rising edge denotes start of octal frame. Input frequency is 44.1Khz or 48Khz.
29	IOBUS_WCLK/	INPUT	Not used
35	IOBUS_64FS/	INPUT	Not used
57	IOBUS_256FS	INPUT	Not used
8	I2S_FS/	OUTPUT	AD Frame Sync – falling edge denotes start of frame. Locally generated.
37	I2S_64FS/	OUTPUT	AD bit clock - falling edge denotes start of bit period. Locally generated.
23	I2S_256FS	OUTPUT	AD MCLK signal. Locally generated. Does not actually scale with sample rate. Nominal output frequency is **XXXX(44.1/88.2Khz) or XXXX(48/96Khz)**

Pin	**Name**	**Type**	Description
Serial Audio			
3	I2S0	OUTPUT	I2S audio data for channel 1
4	I2S1	OUTPUT	I2S audio data for channel 2
5	I2S2	OUTPUT	I2S audio data for channel 3
6	I2S3	OUTPUT	I2S audio data for channel 4
18	I2S4	OUTPUT	I2S audio data for channel 5
19	I2S5	OUTPUT	I2S audio data for channel 6
24	I2S6	OUTPUT	I2S audio data for channel 7
25	I2S7	OUTPUT	I2S audio data for channel 8
20	SDO0	INPUT	TMIX Octal data. Received from TMIX2 Octal 0. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)
14	SDO1	INPUT	TMIX Octal data. Received from TMIX2 Octal 1. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)

7	SDO2	INPUT	TMIX Octal data. Received from TMIX2 Octal 8. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)
84	SDO3	INPUT	TMIX Octal data. Received from TMIX2 Octal 9. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)
9	SDO4	INPUT	TMIX Octal data. Received from TMIX2 Octal 10. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)
10	SDO5	INPUT	TMIX Octal data. Received from TMIX2 Octal 11. Octal selection is determined by the octal select field in the FPGA control register(see register description for details)
Audio Control			
44	DEEPMH	OUTPUT	Deemphasis control. Enabled when asserted(1).
39	RLY_MUTE/	OUTPUT	Relay Mute Control. Analog outputs are muted when asserted(0)
27	DAMUTE	OUTPUT	DA Mute. Digital output from DA is muted when asserted(1)
28	DAC_RST/	OUTPUT	DAC reset. All DACs' are reset when asserted(0).
26	96K_EN	OUTPUT	96K sample rate enable. DACs' operate in 2x(88.2/96K) sampling mode when asserted(1).
Charge Pump Support			
38,36, 58	VBOSCU/,VBOSCD/, VCCOSC	OUTPUT	Charge pump clock signals
FPGA Support			
32	MODE	INPUT	MODE - Serial download interface mode signal. Nomimally zero for loading from external SPROM
55	PROG/	INPUT	FPGA Program. 0 : causes the FPGA to reload its program from the external SPROM.
73	CCLK	OUTPUT	CCLK . Serial PROM clock signal
53	DONE	OUTPUT	FPGA DONE - Asserted when FPGA program cycle has completed.
41	INIT/	OUTPUT	FPGA serial download initialization signal.
71	DIN	INPUT	FPGA configuration data from SPROM
15,16, 17	TDI,TCK,TMS	INPUT	JTAG Interface. Not used
75	TDO	OUTPUT	JTAG Interface. Not used

Power Supply

Power conditioning for the Analog Output card involves local filtering and regulation of supplies from the backplane, as well as the production of boosted voltages for special purposes.

The main 5VD from the backplane is used by the fpga and the digital sections of the D/A converters.

The 12V supplies from the backplane (+12VSUP/-12VSUP) are filtered by FB4/FB1 and associated capacitors to supply +/-12V to the analog op-amps. +12VSUP also supplies U3 through a string of 5 dropping diodes to provide regulated +5VA for the D/A converters, which consume 8 x 15=120mA maximum. Diodes D8, D9 prevent large differences from existing between the 5V pins of the converters.

U4 develops regulated 6.6V from +12VSUP, through 3 shared dropping diodes. This voltage supplies U5, which is the switching device for the VCC charge pump. U5 switches at 64FS (in the range of 3-6MHz), driving a low-impedance square wave into circuitry consisting of schottky diodes and associated capacitors. This boosts the +/-12V to create supplies of around +/-18V, which vary some with load due to the impedance exhibited by the switch and diodes.

Dropping diodes in series with regulators U3 and U4 reduce their operating voltage, resulting in cooler operation.

Bias voltage VB is derived from both +/-12VSUP by switching transistors Q1,Q2 and associated diodes and capacitors. An ac coupled two-phase clock at wordclock rate drives the transistors with non-overlapping on-times creating a 24V squarewave to augment the +12V, which in a perfect pump would make VB=36V, neglecting losses. In practice, VB is somewhat over 30V at its normal load of approximately 40mA (16*2.4mA).

AES card

Introduction

This section describes the theory of operation of the 960L AES card.

Overview

The 960L AES Card supports eight channels of AES digital audio I/O at 44.1KHz/48KHz and 88.2 KHz/96 kHz. The AES inputs are received using four Crystal CS8413 digital audio receivers and the outputs are driven with four CS8403A digital audio transmitters. The receivers pass I2S audio to the AES FPGA, which packs the eight samples into octal serial streams that interface to the Reverb Card via the I/O Bus. The transmitters receive I2S audio from the FPGA. These I2S streams are unpacked from octal serial streams that are sent from the Reverb Card. The FPGA contains control and status registers as do the AES devices, which are accessed by the Reverb Card via the I/O Bus.

Figure 1-1 is a block diagram of the 960L AES card.

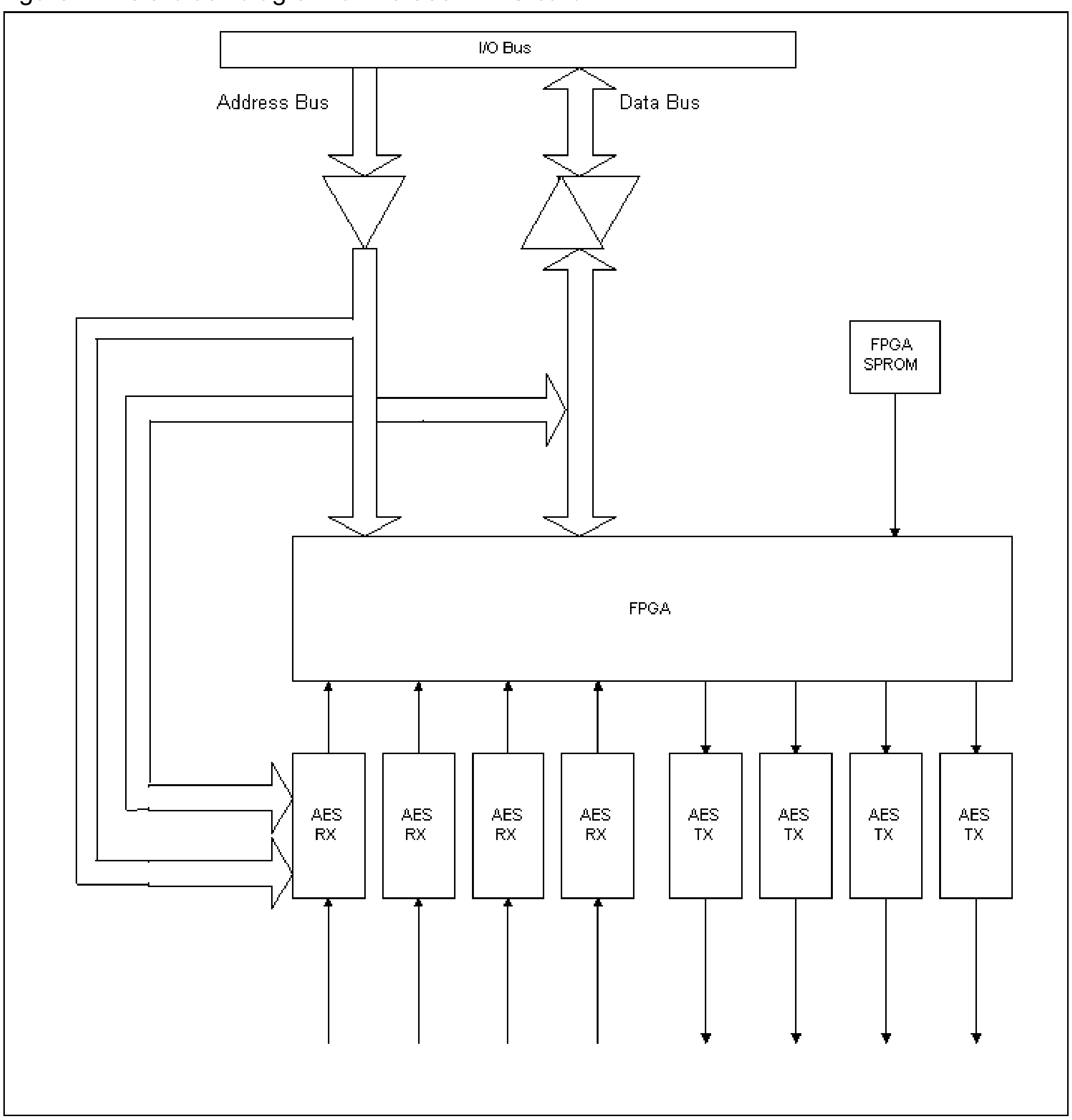


Figure 1-1 AES Card Block Diagram

Circuit Description

This section is a page by page description of the 960L AES card schematic.

Crystal RX/TX Devices (sheets 1-4)

Sheet 1 of the schematic shows a single Crystal receiver and transmitter and associated support circuitry. Sheets 2, 3, and 4 are the other receivers and transmitters. The description of sheet 1 also applies to sheets 2, 3, and 4. Digital audio is received through an XLR connector (J3). This differential pair is transformer coupled by TX2 and terminated by R38 before being presented to the Crystal CS8413 digital audio receiver (U6). The device has a microprocessor interface and internal registers that are used to configure the device and to monitor the status of incoming digital audio stream. Digital audio is transmitted by the Crystal CS8403A digital audio transmitter (U10). This device also has a microprocessor interface and internal registers that are used to configure the device. The differential output from this device is transformer coupled through TX10 and transmitted through an XLR connector (J7).

FPGA (sheet 5)

The primary function of the AES FPGA (U2) is to convert octal format serial audio to I2S format in the following manner. The Crystal receivers pass I2S audio to the AES FPGA that packs the eight samples into octal serial streams that interface to the Reverb Card via the I/O Bus. The Crystal transmitters receive I2S audio from the FPGA. These I2S streams are unpacked from octal serial streams that are sent from the Reverb Card. The FPGA also contains control and status registers to set up and monitor the card's operation. These registers are described in sections 5 – 10 of this document. At start-up the FPGA clocks in its configuration program from a serial PROM (U3).

I/O Bus Buffers (sheet 6)

The buffers to interface the AES card to the I/O Bus are shown on sheet 6.

I/O Bus Connector (sheet 7)

The I/O Bus connector (J1) is a 96 pin Euro DIN connector that is used to interface the AES card to the Reverb Card.

Bypass Caps and Ground Jumpers (sheet 8)

The chassis ground - signal ground jumpers shown on sheet 8 should be installed to connect chassis ground to signal at the AES card to meet EMC requirements.

Startup Sequence

At power-up the AES FPGA clocks in serial configuration data from its companion SPROM. This program is used by the FPGA to configure its internal gates and memory to perform the desired functions for the AES card. After the FPGA has successfully configured itself it illuminates the DONE LED (D1, sheet 6). The AES card is now ready to respond to a request from the Reverb Card to identify itself. This process consists of the Reverb Card reading the configuration register in the AES FPGA, which is set a value of 32 hex. This tells the Reverb Card that this is an AES card in this slot on the I/O bus, and the Reverb Card then programs the FPGA registers and the registers in the Crystal devices for card to operate. The AES card is accessed periodically by software during normal operation to poll the status of the incoming AES audio/data streams for errors, and the Reverb Card also accesses the AES card registers to perform the sequence required when locking the 960L sample clock to an AES input. The sequence is described in section 7 of this document.

AES card Memory Map

Address	Resource

BASE+1E0	Crystal AES TX #4
BASE+1C0	Crystal AES TX #3
BASE+1A0	Crystal AES TX #2
BASE+180	Crystal AES TX #1
BASE+160	Crystal AES RX #4
BASE+140	Crystal AES RX #3
BASE+120	Crystal AES RX #2
BASE+100	Crystal AES RX #1
BASE+80	Octal Select Register
BASE+60	Crystal AES TX global chip select (used for synchronized TX reset)
BASE+40	Lock Register
BASE+20	FPGA Control Register
BASE+00	Board I.D. register (read only, hardwired to $33)

FPGA Control Register

Register Bit Number	Function	Active State
7	Bit 1 of encoded source for slot word clock output	See following table
6	Bit 0 of encoded source for slot word clock output	See following table
5	Bit 1 of encoded source for preview word clock output	See following table
4	Bit 0 of encoded source for preview word clock output	See following table
3	Slot word clock output enable	High
2	Preview word clock output enable	High
1	Double speed mode	High
0	Local loopback mode (for test only)	High

Hex value	Selected Word Clock Source
3	AES input #4
2	AES input #3
1	AES input #2
0	AES input #1

FPGA Lock Register

Register Bit Number	Function	Active State
7	(not used)	-
6	(not used)	-
5	(not used)	-
4	(not used)	-

3	(not used)	-
2	(not used)	-
1	Enter word clock seek mode (see following discussion)	high
0	Drive clocks to Crystal receivers (see following discussion)	high

Locking to the AES Input Word Clock

The procedure to derive the system word clock from an AES input stream is as follows:

1. Set bit 0 of the Lock Register low and bit 1 high to enter seek mode.
2. Program the selected Crystal AES receiver to be in master mode by setting bit 1 of the receiver's Control Register 2 high. Bit 2 of the Interrupt Enable register of all of the Crystal receivers should also be set high.
3. Wait at least 10 mSec.
4. Set bit 1 of the Lock Register low to exit seek mode.
5. Program the selected Crystal AES receiver to be in slave mode by setting 1 of the receiver's Control Register 2 low.
6. Set bit 0 of the Lock Register high to drive clocks to the Crystal receivers. The system is now locked the selected AES stream. If the cable is disconnected or the sample rate is out of range then this procedure will need to be repeated to reestablish lock. Software should monitor the loss of lock status in the selected AES receiver to detect loss of AES signal, and should also monitor slipped sample to detect an input stream that is out of the accepted sample rate range.
7. Global TX Reset Chip Select

This address is decoded as a simultaneous chip select for all four Crystal AES transmitters. This location should be used to reset all four devices within the same word clock period. This technique will ensure that the AES transmitters' NRZI streams are aligned properly.

Octal Select Register

Register Bit Number	Function	Active State
7	Not used	-
6	Not used	-
5	Not used	-
4	Output octal group = Tmix #1 Octals 0 & 1	High
3	Output octal group = Tmix #1 Octals 10 & 11	High
2	Output octal group = Tmix #1 Octals 2 & 3	High
1	Input octal group select encoded bit 1	See following table
0	Input octal group select encoded bit 0	See following table

Hex value	Selected Input Octal Group
3	(not used)
2	Tmix #2 Octals 8 & 9
1	Tmix #2 Octals 10 & 11
0	Tmix #2 Octals 2 & 3

Local Loopback Mode:

When the local loopback mode bit is set in the FPGA control register, the AES inputs are looped through the FPGA and back to the AES outputs. Also, the octal data received from the Reverb card is looped back to the Reverb card by the FPGA as follows:

TMIX #2 octals 2 & 3 to TMIX #1 octals 10 & 0
TMIX #2 octals 8 & 9 to TMIX #1 octals 2 & 3
TMIX #2 octals 10 & 11 to TMIX #1 octals 11 & 1

Reverb card

Introduction

This section describes the theory of operation of the 960L Reverb Card.

Overview

The 960L Reverb Card is a 128 channel, 24 bit audio DSP processor that is the central DSP resource in the 960L system. Up to three of these cards can be inserted into the PCI bus for mixing, effects, and other processing needs. The card has four Lexichip III reverb processors which are controlled by two Z-80 microprocessors. Audio mixing and the host interface are implemented with a Motorola 56301 DSP microprocessor. Digital audio data is transferred to and from the card via the 960L I/O bus by two T-MIX serial audio engines ASICs. The host Pentium microprocessor controls the I/O peripheral cards in the 960L by sending commands through the Reverb card to the I/O bus. A third T-MIX ASIC is used to transfer serial digital audio to and from the four Lexichip III chips. The 56301 reads and writes audio samples to the T-MIX devices via a high-speed 24-bit data path.

Figure 1-1 is a block diagram of the 960L Reverb Card.

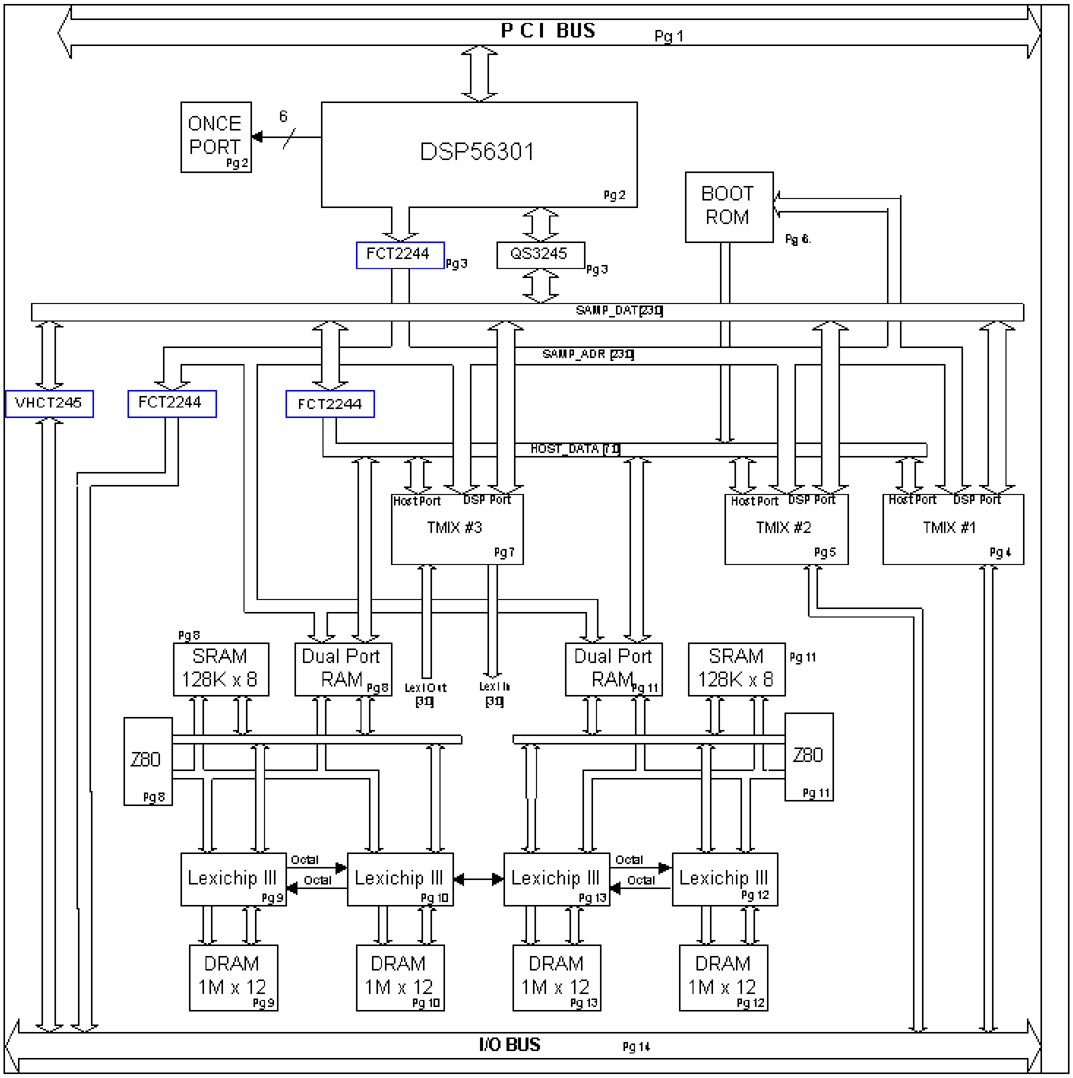


Figure 1-1 Reverb Card Block Diagram

Circuit Description

This section is a page by page description of the 960L Reverb Processor schematic.

PCI Bus (sheet 1)

The PCI bus is a 33 MHz, 32 bit multiplexed address/data bus that serves as the interface between the Reverb Card and the host Pentium processor. The DSP 56301 provides an integrated, glue-less interface to the PCI bus including all of the configuration and address mapping registers. Master and slave modes are supported. The Reverb card requires 12V, 5V, and 3.3V.

56301 DSP Microprocessor (sheet 2)

The 56301 operates at 3.3V which is provided by the PCI connector. The 56301 is clocked from an external 6 MHz crystal (Y1, sheet 2) and the on-chip PLL is used to generate an 80 MHz clock which is output as DSP_CLKOUT. The reset control chip (U37) creates a reset pulse with a minimum duration of 20ms as required by the 56301. The Once Port is used for development and is not populated for production cards. The 56301 moves samples to/from the T-MIX devices and its internal memory using the DSP bus, which appears on the right hand side of the chip symbol. The DSP56301 has internal address decoders that are

used to generate the AA0/, AA1/, AA2/, and AA3/ chip select signals. These address decodes are assigned to:

AA0/ – I/O BUS (16 wait states)
AA1/ – T-MIX Host bus, Dual Port Ram, Boot PROM (8 wait states)
AA2/ – T-MIX devices DSP bus (3 wait states)
AA3/ – (Not Used)

DSP 56301 Interrupts

The 56301 external interrupts are assigned as follows:

- IRQA – Word Clock Interrupt
- IRQB – I/O Bus Interrupt (not used)
- IRQC – Dual Port Ram Interrupt from Z80 1
- IRQD – Dual Port Ram Interrupt from Z80 2

56301 SCLK Output

The 56301 SCLK output is used to supply a clock to the T-MIX devices at start-up through the mux (U45) on sheet 15. This clock is needed at start-up because the TMIX_CKI signal may not be available when the T-MIX devices are initialized. After the TMIX_512FS signal becomes available the 56301 switches the mux.

DSP 56301 Timers

The 56301 has three timers that use the pins TIO0, TIO1, TIO2. TIO0 receives the PREVIEW_CLKS signal, which is a word clock signal that is sourced from any of the available word clock sources in the 960L. The timer measures this signal and the result is used by software to determine if the selected word clock frequency is acceptable. This clock is not necessarily the one the system is currently using. TIO1 receives the TOT_WCK signal, which is the word clock the system is currently using. TIO2 is a watchdog timer output from the 56301.

56301 Data & Address Buffers (sheet 3)

The DSP bus is used by the 56301 to access the T-MIX devices, the Z80s, and is the pathway to the I/O bus. The DSP data bus interface to the 56301 uses 3.3V logic levels. The 56301 address bus also drives 3.3V logic levels. The 56301 control bus drives 3.3V logic levels, but control inputs to the 56301 are tolerant of 5V logic levels. 5V/3V interface devices are required to interface the 56301 to the T-MIX devices since these Asics have 5V CMOS inputs and outputs. The 5V/3V level translation is accomplished by using Quickswitch QS2345 bus switches to attenuate 5V signals to 3V levels These devices are U10, U11, and U12 on sheet 3. These devices will attenuate the 5V signals provided they are powered by a 4.3V source, which is provided by an adjustable regulator (U2, sheet 14). The T-MIX devices must have 5V CMOS levels on their input pins, so the 3V signals from the 56301 must be converted to 5V CMOS logic levels, This is done using FCT2244 buffers (U4, U5, U6, U7, U8, U9, U13, U14 on sheet 3). Pull-up resistors are used on the SAMP_DAT5V bus to set the data bus to a valid logic level when the bus drivers are tri-stated.

T-MIX #1 (sheet 4)

The Reverb Card has three T-MIX devices. These chips function as serial to parallel converters for digital audio. The 56301 transfers 24 bit parallel audio samples to/from the T-MIX chips. T-MIX #1 shown on sheet 4 receives serial digital audio from audio input cards on the I/O bus. These digital audio streams are formatted with eight audio samples per word clock. These audio streams can be probed on R126-R138, and if a scope is triggered on word clock it is possible to see the audio samples in these data streams. The assignment of these signals to the I/O cards in the system is under software control and changes depending upon how the I/O bus is populated. The TMIX1_NSAC signal is the audio word clock interrupt to the 56301.

T-MIX #2 (sheet 5)

T-MIX #2 shown on sheet 5 sends serial digital audio to audio output cards on the I/O bus. These digital audio streams are formatted with eight audio samples per word clock. These audio streams can be probed on R146-R157, and if a scope is triggered on word clock it is possible to see the audio samples in these data streams. These signals represent digital audio that has been processed by the Reverb Card, and when monitored in conjunction with the signals on T-MIX #1 are an indicator of the end-to-end integrity of the Reverb Card's audio processing chain. The assignment of these signals to the I/O cards in the system is under software control and changes depending upon how the I/O bus is populated. The SPO0-7 signals on the T-MIX are general-purpose I/O pins, which are used to drive the signals DBRD_RST0/ and DBRD_RST1/. These are the reset signals to the Lexichips.

Gals (sheet 6)

The logic to interface the 56301 to its on-board peripherals is shown on sheet 6. The 56301 Strobe Control GAL (U19) creates the strobes that interface to the T-MIX control ports (SAMP_RD/, TMIX_WR/, TMIX_HWEN/). It also generates the sample bus data transceiver control signals (SAMP_RD/ and SAMP_WR/). The TMIX_HRDY/ signal is used to extend 56301 data transfer cycles as required by the T-MIX chips. This signal is qualified with the CTRL_SEL/ chip select in this GAL to create the TRANS_ACK/ signal to the 56301. When the TMIX_HRDY/ signal is high and CTRL_SEL/ is low, TRANS_ACK/ is high and the data transfer cycle is extended.

The 56301 Decode GAL (U17) generates the chip selects for the T-MIX DSP ports (TMIXn_DSP_CS) and it creates the dual port RAM chip selects, read strobes, and write strobes (DP_RAMn_CS/, DP_RAM_RD/, and DP_RAM_WR/).

The Tmix Chip Select GAL (U16) generates the T-MIX control port chip selects (TMIXn_CTL_CS/), the Boot PROM chip select (BOOT_SEL/), and the T-MIX DSP port interface clock (TMIX_DCLK).
The Boot PROM (U18) is used by the 56301 to get its start-up configuration. This information consists of the 56301 clock PLL multiplier value, which is used to multiply the 6 MHz clock to 80 MHz, and the PCI subvendor I.D. that is passed to the host Pentium processor as part of the start-up process.

The DSP Interrupt Buffer (U3) is tri-stated at start-up to allow the resistors R36-39 to drive the dual function interrupt/mode signals to the 56301. When the 56301 senses the rising edge of the DSP_RESET/ signal it samples the IRQA/, IRQB/, IRQC/, and IRQD/ signals to determine the boot mode it should use. These resistors set the 56301 to boot from the Boot PROM (U18). After the 56301 is initialized it enables the DSP Interrupt Buffer using the IRQ_EN/ signal, which passes the interrupt requests to the 56301.

T-MIX #3 (sheet 7)

T-MIX #3 shown on sheet 7 transfers serial digital audio to the four Lexichips on the Reverb Card. These digital audio streams are formatted with four audio samples per word clock. These audio streams are the LEXI_n_SER_IN and the LEXI_n_SER_OUT signals. The LEXI_WCLK_IN signal driven from U38 is the word clock signal for the four Lexichips. The SPO0-7 signals on the T-MIX are general-purpose I/O pins that are used to drive the signals Z80_INIT1/ and Z80_INIT2/. These are the reset signals to the Z80 microprocessors. The Z80-Lexichip Interface GAL (U26) contains the glue logic to connect the Z80s to the Lexichips. It generates chip select and memory request signals and also generates the ZWAIT1/ and ZWAIT2/ signals which are signals that are sent to the Z80s to extend data transfer cycles as required by the Lexichips.

Z-80 #1 (sheet 8)

Z80 #1 and its associated local SRAM and dual port SRAM are shown on sheet 8. This Z80 (U33) is the control processor for the Lexichip #1 & #2 reverb engines (U40, U46). Its address and data lines are connected directly to both the local SRAM and dual port SRAM, and the chip selects for these SRAMs are generated by Lexichip #1 (DPORT_1_CS/, SRAM1_CS/). The dual port SRAM is initialized with the Z80 start-up code by the 56301 using the port shown on the right-hand side of the chip symbol. The Z80 accesses this SRAM using the port on the left-hand side of the chip symbol. Message passing between the

56301 and the Z-80 is also accomplished through this dual port SRAM. Address $7FF in the dual port SRAM is used to generate an interrupt to the 56301 (DB_MAS_INT0/). The 56301 then reads this address which is written with interrupt vector data by the Z-80. The interrupt is cleared when this address is read by the 56301. In a similar fashion, address $7FE in the dual port SRAM is used by the 56301 as an address to create an interrupt to the Z-80 (MAS_DB_INT0). The description of this page also applies to Z80 #2 and its associated SRAM shown on sheet 11.

Lexichip #1 (sheet 9)

Lexichip #1 (U40) and its associated DRAM (U41) are shown on sheet 9. Lexichip processes serial digital audio that is received on the LEXI1_SER_IN signal that is sent from T-MIX #3. Serial digital audio is passed from Lexichip #1 to Lexichip #2 through the LEXI1_TO_LEXI2_SER signal, and serial audio is returned via the LEXI2_TO_LEXI1_SER signal. Finally, serial audio is returned after processing to T-MIX #3 on the LEXI1_SER_OUT signal, completing the audio data path through this group of two Lexichips. Serial audio is shifted in and out of the Lexichips using the LEXI_256FS clock signal. All four Lexichips receive the 12MHZ clock signal and multiply this clock to 50MHz for internal use using an on-board PLL. The PLL filter for Lexichip #1 is comprised of R93, R94, and C56. The PLL supply voltage is filtered by R88, C54, and C22. The DRAM is used by Lexichip to store audio samples for processing. The Z1_DATA bus has resistors (R65-91) which drive the bus at start-up since all other data bus drivers are tri-stated at this point. Lexichip #1 and #2 sample the data bus on the rising edge of DBRD_RST0/ to determine the mode in which they are to be configured.

The Z80-Lexichip Clock GAL (U35) generates the 12MHZ Lexichip clock and the clocks for the Lexichip's Z80 interfaces (ZCLKn) as well as the clock for both Z80s (Z80_CLK). This description of this page also applies to Lexichip #2, #3, and #4 and their associated DRAMs, which are shown on sheets 10, 12, and 13.

I/O Bus Connector (sheet 14)

The Reverb Card passes commands and status between the host Pentium processor and the I/O Bus peripheral cards through the I/O bus connector (P2).

I/O Bus Control (sheet 15)

The I/O Bus interface is controlled by the 56301 through the circuitry shown on sheet 15. The Lexibus Control GAL (U20) is configured as a counter that is used by the Lexibus Strobe GAL (U23) to create I/O Bus data transfer cycles. The I/O Bus control signals consist of an address strobe (IO_AS/), data strobe (IO_DS/), and read/write qualifier (IO_WR/). (The IO_RD/ signal is no longer used.) Only one of the Reverb Cards in a 960L can serve as the I/O Bus master, so all control signals are only driven if ENAB_IOBUS/ Is low, otherwise all I/O Bus outputs from the card are tri-stated. The ENAB_IOBUS/ signal is controlled by the Pentium host software through the 56301. I/O bus data is transferred through U39, and the I/O Bus address is driven through U31, U32, and U44. Provisions for a serial EEPROM on the I/O Bus backplane are supported by the control signals driven through U50. The IOBUS_INT/ shown on U30 is a wire-ored interrupt signal from the I/O Bus that is not currently used. The Audio Clock Mux (U45) is used to provide clocks to the T-MIX devices at start-up. The start-up clocks are INIT_CLK and WCLK. After initialization of the 960L Clock/IO card the TMIX_CKI and TMIX_WCKI signals are active and the mux is switched to use these clocks for the T-MIX devices.

Startup Sequence

At power-up the 56301 is held in the reset state by the power supply monitor (U37, sheet 1) for a minimum of 20 ms after +5VD has stabilized. Once the DSP_RESET/ signal has gone high the 56301 will exit the reset state and read its bootup program from the Boot PROM (U18, sheet 6). If the bootup procedure completes successfully then the clock measured on R168 will be 80 MHz. If the 56301 failed to boot correctly this clock will be 3 MHz. After the 56301 has completed its bootup procedure it waits for a startup program to be sent through the PCI interface. This startup program is sent when the host system is starting the Windows operating system. If this program is received and executed correctly the DSP LED is illuminated. Once the 960L application is launched another 56301 program is sent from the host computer.

Upon receipt of this program the 56301 initializes the three T-MIX devices and loads a program into the Z-80 dual port RAMs. The 56301 releases the Lexichips and Z-80s from the reset state by driving the DBRD_RSTn/ signals high and the Z80_INITn/ signals high. At this point the Z-80s execute their startup code from the dual port RAMs and pass messages back to the 56301 using the DB_MAS_INTn/ interrupt signals and the dual port RAM interrupt vector locations. The Z-80s will illuminate the Z-80 LEDs under software control to indicate their startup success or failure. The 56301 then receives commands from the host to detect which cards are resident on the 960L I/O bus. After reporting this information to the host processor through the PCI bus the 56301 is commanded by the host to initialize the cards resident on the 960L I/O bus.

DSP 56301 Expansion Port Memory Map

Address Attribute Number	Address	Resource
-	$FF0000 - $FFFFFF	Internal Decodes
AA1	$D00400 - $FEFFFF	-
AA1	$D00000 - $D003FF	Boot PROM
	$9D8000 - $CFFFFF	-
AA1	$9D4002 - $9D7FFF	-
AA1	$9D4001	T-mix #3 Control Data Port
AA1	$9D4000	T-mix #3 Control Pointer Port
AA1	$9D3002 - $9D3FFF	-
AA1	$9D3001	T-mix #2 Control Data Port
AA1	$9D3000	T-mix #2 Control Pointer Port
AA1	$9D2002 - $9D2FFF	-
AA1	$9D2001	T-mix #1 Control Data Port
AA1	$9D2000	T-mix #1 Control Pointer Port
AA1	$9D1800 - $9D1FFF	-
AA1	$9D1000 - $9D17FF	Dual Port SRAM #2
AA1	$9D0800 - $9D0FFF	-
AA1	$9D0000 - $9D07FF	Dual Port SRAM #1
AA1	$9C0001 - $9CFFFF	-
AA1	$840000 - $9BFFFF	-
AA2	$83C400 - $83FFFF	-
AA2	$83C000 - $83C3FF	T-mix #1 DSP Port
AA2	$83A400 - $83BFFF	-
AA2	$83A000 - $83A3FF	T-mix #2 DSP Port
AA2	$838400 - $839FFF	-
AA2	$838000 - $8383FF	T-mix #3 DSP Port
AA2	$800000 - $837FFF	-
	$308000 - $7FFFFF	-
AA0	$301A00 - $307FFF	-
AA0	$301800 - $3019FF	IOBUS SLOT #5-
AA0	$301600 - $3017FF	IOBUS SLOT #4
AA0	$301400 - $3015FF	IOBUS SLOT #3
AA0	$301200 - $3013FF	IOBUS SLOT #2
AA0	$301000 - $3011FF	IOBUS SLOT #1-
AA0	$300000 - $300FFF	-
	$010000 - $2FFFFF	-
	$0 - $00FFFF	Internal Decodes

Z80 Memory Map

(same for both Z80s)

Address	Resource
$0 - $7FE	2K Dual Port SRAM
$7FF	Motherboard interrupt mailbox
$3000 - $3BFF	Lexichip #1 internal decodes
$4000 - $7FFF	4 banks of 16K bank-swapped SRAM
$8000 - $8BFF	Lexichip #2 internal decodes
$C000 - $FFFF	4 banks of 16K bank-swapped SRAM

Larc2

This section describes the theory of operation of the LARC2 main board and related modules. Refer to Lexicon schematic 060-13379.

General Description

The LARC2 is the remote control unit for the Lexicon 960L Digital Effects System. LARC2 provides easy access to all of the 960L functions and parameters. A thin cable provides a direct link with the mainframe from up to 50 feet away or up to 1000 feet with an external12VDC power supply.

The LARC2 system board contains the following standard components:

- Intel SA-1100 Processor
- 64KBytes Boot ROM
- 8 Mbytes of Flash
- 16 Mbytes of EDO DRAM
- Control for 8 motorized faders
- Control for an 640 x 240 LCD display
- Keypad and serial interfaces
- Diagnostic LEDs

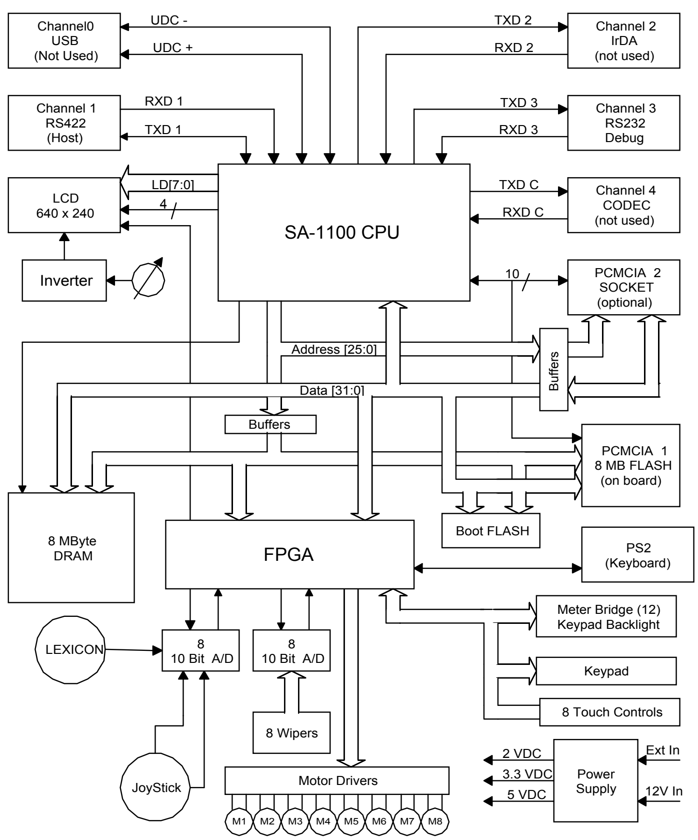


Figure 1-1 LARC2 Block Diagram

Central Processor (sheet 1)

The system central processor is a highly integrated microprocessor that incorporates a 32-bit StrongARM RISC processor core, system support logic, multiple communication channels, an LCD controller, a PCMCIA controller, and general-purpose I/O ports.

Processor Summary (U8, sheet 1)

The SA-1100 Microprocessor is a general-purpose, 32 bit RISC microprocessor with the following features:

- 16 Kbyte instruction cache
- 8 Kbyte write-back data cache
- 512 byte mini data cash that allocates data based on the MMU
- 4 entry read buffer and an 8 entry write buffer
- Integral memory management unit (MMU)

The logic outside the core and caches is grouped into the following three modules:

- Memory and PCMCIA control module (MPCM)
- Memory interface supporting ROM, Flash, DRAM, SRAM, and PCMCIA control signals

- System control module (SCM)
- Twenty-eight general purpose I/O ports (interrupt capable)
- Real-time clock, watchdog, and interval times
- Power management controller
- Interrupt controller
- Reset controller
- Two on-chip oscillators for connection to 3.686 MHz and 32.768 kHz crystals

- Peripheral control module (PM)
- Six-channel DMA controller
- Gray/color, active/passive LCD controller
- 230 Kbps SDLC controller
- 16550 compatible UART
- IrDA serial port (115 Kbps, 4 Mbps)
- Synchronous serial port (UCB1100, UCB1200, SPI, TI, uWire)

Memory Map

Table 2-1 shows the memory SA-1100 memory map. The map is divided into four main partitions of 1 Gbyte each.

Base Address	SA-1100	LARC2
0xE800 0000	Reserved	
0xE000 0000	Zeros Bank	
0xD800 0000	DRAM Bank 3	Not used
0xD000 0000	DRAM Bank 2	Not used
0xC800 0000	DRAM Bank 1	Not used
0xC000 0000	DRAM Bank 0	DRAM bank 0
0x8000 0000	Internal Registers	
0x4000 0000	Reserved	
0x3000 0000	PCMCIA Socket 0	8 Mb Flash (alternate)
0x2000 0000	PCMCIA Socket 1	Optional PCMCIA Socket

Base Address	SA-1100	LARC2
0x1800 0000	Static Bank Select 3	Configuration Register
0x1000 0000	Static Bank Select 2	LARC2 Registers
0x0800 0000	Static Bank Select 1	8 Mb Flash
0x0000 0000	Static Bank Select 0	Boot ROM

Table 2-1 LARC2 Memory Map

The bottom partition (0x0000 0000 to 0x3FFF FFFF) is dedicated to static memory devices (ROM, Flash, SRAM) and to the PCMCIA expansion bus area. This space is divided into four 128 M byte blocks for static memory devices and two 256 Mbyte blocks for PCMCIA.

The next partition (0x4000 0000 to 0x7FFF FFFF) is reserved. Accessing this reserved space results in a data abort exception.

The third partition (0x8000 0000 to 0xBFFF FFFF) contains all on-chip registers. This block is further subdivided into four blocks of 256 M-bytes each. They contain the control registers for the major functional blocks within the chip. The LCD and DMA controllers occupy the top 256 M-byte partition.

The fourth partition (0xC000 0000 to 0xFFFF FFFF) contains DRAM memory. The bank sizes for DRAM are fixed at 128 Mbyte each. The next 256 Mbyte block in this partition is mapped within the memory controller and returns zeros when read. This function is intended to facilitate rapid cache flushing by not requiring an external memory access to load data into the cache. Writes to this space have no effect. The top 384 M-byte of this partition is reserved. Accessing this space causes a data abort exception.

Reset Controller (U5, sheet 1.)

When power is applied, U5 (DS1233) asserts RESET/ and monitors the rise of the 3.3V logic supply. Once it rises above 2.97V (within 10% of 3.3 V), RESET/ remains asserted for an additional 350msec, allowing circuitry to stabilize at nominal operating voltage in the reset state.

When the RESET/ signal is asserted low, SA-1100 stops executing instructions, asserts the RESET_OUT/ pin, and then performs idle cycles on the bus.

When the RESET/ is negated, SA-1100 does the following:

1. Forces the internal program counter to fetch the next instruction from address 0h0000 0000.

2. Based on the state of ROM_SEL pin, fetches the instruction from either 16-bit (ROM_SEL low) or 32-bit space (ROM_SEL high).

Main Memory (sheet 2)

DRAM (U11, U17, sheet 2)

LARC2 uses two 64 Mbyte, 60 ns EDO DRAM chips organized as 1 bank x 4 M Words x 32 bits giving the system 16 MBytes of DRAM. The memory occupies address space 0xC000 0000 to 0xC0FF FFFF. The following table lists the memory transactions that are supported.

Bus Operation	Burst Size	Starting Address Bits [4:2]	Description
Read single	1	Any	Generated by core, DMA or read buffer request.

Read burst	4	0 4	Generated by read buffer or DMA request.
Read burst	8	0	Generated by cache line fills or read buffer requests.
Write single	1	Any	1..4 bytes are written as specified by byte mask. Generated by write buffer or DMA request.
Write burst	2	0, 1, 2, 4, 5, 6	All four bytes of each word are written. Generated by write buffer or DMA request.
Write burst	3	0, 1 4, 5	All four bytes of each word are written. Generated by write buffer or DMA request.
Write burst	4	0 4	All four bytes of each word are written. Generated by write buffer or DMA request.
Write burst	8	0	Cache line copyback. All 32 bytes are written.

Table 3-1 SA-1100 Transactions

Refresh timing

The SA-1100 provides support for a CAS before RAS (CBR) refresh cycle which is shown below.

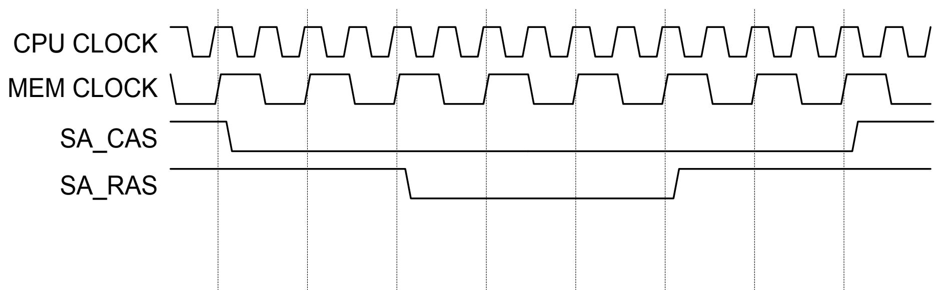
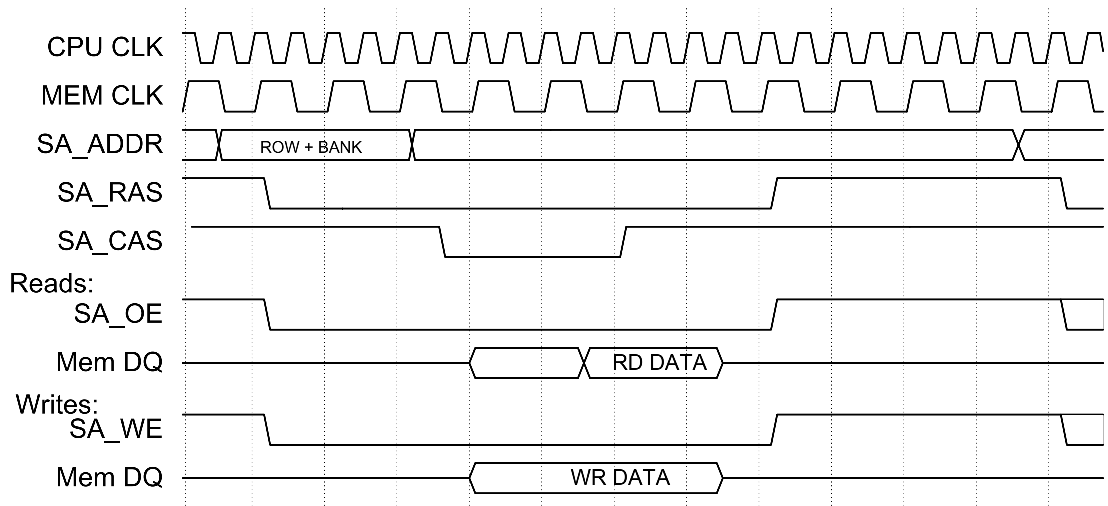


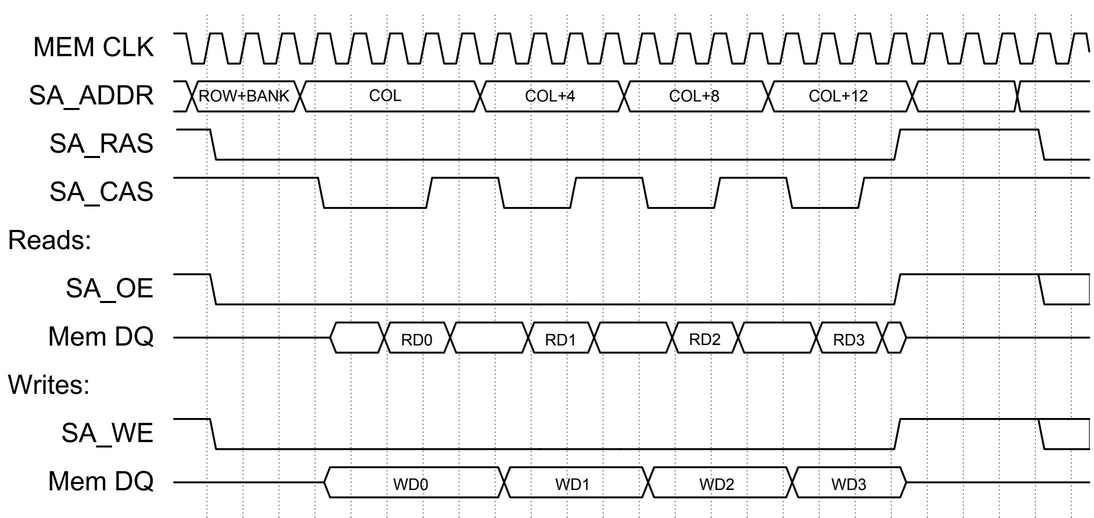
Figure 3-1 Refresh Timing

Read-Write timing



MDCAS0 = 1100 0001 1111 0000 0111 1100 0001 1111
MDCAS1 = 1111 0000 0111 1100 0001 1111 0000 0111
MDCAS2 = 1111 1111 1111 1111 0000 0111 1100 0001
MDCNFG:TRP=4 MDCNFG:CDB2 = 0 TDL=00

Figure 3-2 Dram Single Transactions



Last <--
MDCAS1=1100 MDCAS0=1100 1100 1100 1100 1100 1100 1100 0111
MDCNFG:TRP=4 MDCNFG:CDB2 = 0 TDL=00

Figure 3-3 Dram Burst Transactions

Boot Flash (U12, sheet 2)

The Boot Flash is a 1 Mbit 3 Volt Flash memory organized as 64 k words by 16 bits. The chip is mounted in a 44-pin PLCC socket. The Boot Flash is programmed prior to insertion onto the board but there is code in the Boot Flash to perform updates to the code. The memory is not byte-writeable and must be programmed on a half word boundary (16 bits).

Boot Flash memory occupies address space: 0x0000 0000 to 0x0001 FFFF.

Program Flash (U10, U13, U14, U16, sheet 2)

The program Flash uses the PCMCIA socket 0 interface. It can also be addressed through CS1 address space. This will result in the possibility of having dual entries in the cache. Care should be taken when updating this flash that all entries in the cache are invalidated before doing an update to this Flash. The memory consists of four 16 MBit Flash memory chips. The memory is organized as 2 MBytes by 32 bits. The flash is not byte-writeable and must be written on word boundaries (32 bits).

Program Flash memory occupies address space: 0x0800 0000 to 0x087F FFFF.

Peripheral I/O Subsystems

FPGA, U18 (sheet 3)

The FPGA connects to the cpu address and data buses to interface the cpu with peripheral subsystems. It controls the fader motors, the fader position A/D converters, and the PS-2 keyboard port. Additionally, it acts as a conduit for buffering other peripheral data to the cpu.
These functions are described in the following sections.

Keypad (sheet 8)

The keypad is a rubber assembly containing molded-in conductive pellets. When a key is pressed, its pellet makes a connection between the two halves of a corresponding gold-plated finger pattern on the main pc board. The patterns are organized for scanning as 5 rows by 8 columns. Under software control, the array is scanned by setting one of the row drive lines (RD_KBD [4:0]) to a high level. Each driveline connects to the switch matrix SROW [4:0] through a corresponding diode and resistor (D9-D13, R51-R55). If a keypad switch connected to the driven row is pressed, it connects its row and column, forcing the corresponding bit of the column byte SCOL[7:0] high. Un-driven column bits remain at a low level due to 1K pull-down resistors. A read instruction issued by the CPU asserts the ENA_KBD/ strobe, enabling two 4-bit sections of buffer U24 (74LVC16244) to drive the bidirectional 8-bit LB_D[7:0] bus of FPGA U18. U18 in turn places the byte on the CPU data bus SA_D[7:0] where it is read by the software.

The diodes on the row drivelines prevent multiple simultaneous switch closures from short-circuiting the RD_KBD outputs of U18. Note that in this scanning circuit, two simultaneous switch closures can always be sensed properly; however, this is not true for every combination of 3 or more switch closures because two closures on the same column unavoidably cross-connects two rows, with the result that the other switches on those rows become indistinguishable.

The SA-1100 scans the keypad matrix using 5 address lines. Each address has 8 data bits and is one row within the matrix. A bit that is set to 1 in the register indicates that the key is down.

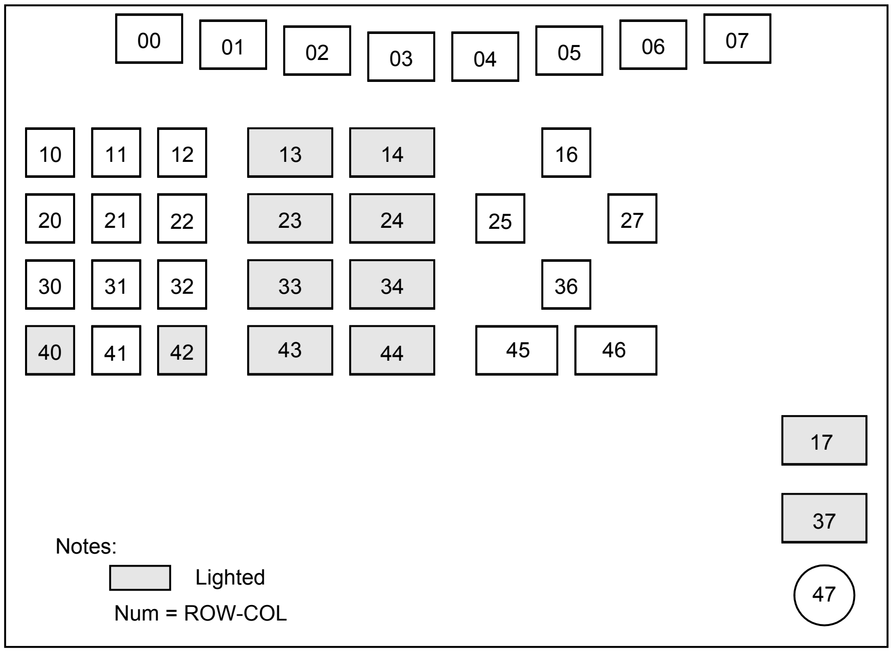


Figure 4-1 Keypad Rows and Columns

Keypad Leds (sheet 8)

There are 12 keys on the keypads that are lighted. The array of LEDs that illuminate the keypad is organized for scanning as 4 rows by 4 columns. Under software control, the array is driven by sequentially saturating one of the four column-driver transistors Q4-Q6. One output of U6 (74AC273) gets set to a logic low to sink base current for one transistor through the associated base resistor R26-R29, while the other three transistor control lines remain high, keeping the other transistors off. The transistor collectors drive the column lines LED_G[3:0], sourcing the anodes of the LEDs the from the 5VD power rail. The cathodes of each column of LEDs connect through current-limiting resistors R22-R25 to the remaining four outputs of U6, the row drivers. Within a driven column, an LED lights when a row driver sinks current from its cathode. Software asserts WR_KPD to load U6 with the appropriate sequence of row and column scanning patterns.

In reset, all LEDs will be lit, because all outputs of U6 are set low, sourcing all anodes via the transistors and sinking current from all cathodes.

A/D Converters

There are two 8-channel 10-bit Analog-To-Digital converters (TLV1548M) on the main board. One is used to get the position of the wiper arm on the 8 faders. The second takes care of the joystick, Lexicon button, and the 12-volt sense.

A single 8-bit command register is implemented to enable the scanning of both A/Ds and to have direct access to the A/D converters. When the enable command is given, the FPGA will do a continuous scan of the inputs storing the values in the FPGA. The addressing of the two converters is interleaved allowing faster updates of the values.

If the scanner is not enabled the command register will allow the selection of a single input or one of the other commands. When the command is given software must wait at least 60 µsecs before reading the value. The value of the selected input is stored in the register locations based on bits [3:0] of the command. This means that one converter will overwrite the locations of the other when in this mode.

4.5. Motorized Faders

Motor Drivers (sheet 5)

The motors on the faders are driven using the raw +12 volts through SGS-Thompson Push-Pull drivers. Software loads an eight word by 32-bit memory array within the FPGA with bit patterns that determine the waveforms that are the inputs to each pair of drivers for each fader. The column of the array is scanned at a programmable clock rate. At the beginning of each column clock the row clock cycles through each row and with the enable bit and the direction bit latches the corresponding output registers to generate an individual differential drive waveform for each motor, the MOTOR + and MOTOR – signals.

At the end of the 32 bit-shifts, the process starts again, forming a continuous train of drive pulses. It is the responsibility of the software to stop the motors by either writing zeros in the enable register or by setting all the memory waveform bits to zero. The MTR_ENAB GPIO bit is a master enable to all motor-driver chips.

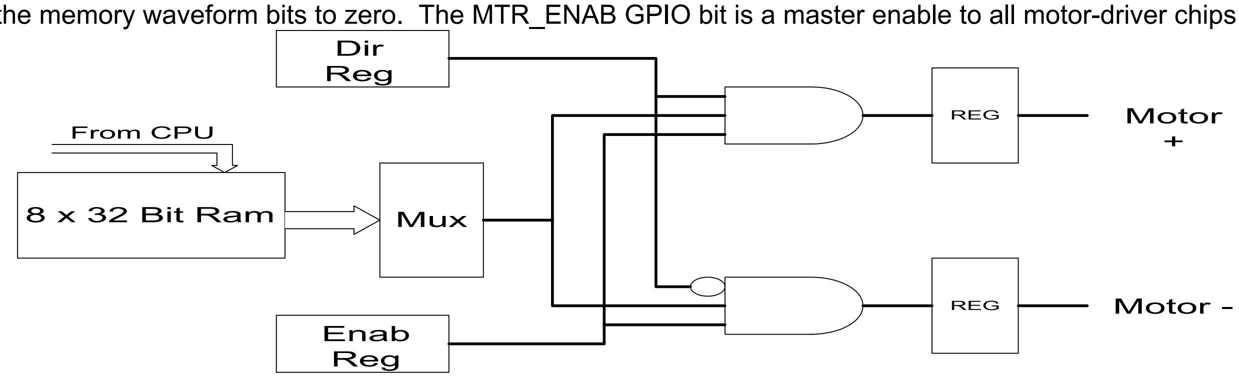


Figure 4-2 FPGA Internal Motor Control Logic

Position Sensing (sheet 5)

Each motorized fader is based on a 10K linear sliding potentiometer. Each potentiometer is connected to a dc source (5VA) and produces a 0-to-5V dc voltage proportional to its position. To digitize the position information, each voltage is fed to one channel of A/D converter U30. The serial port of the converter is scanned under the control of FPGA U18. U18 supplies the serial input to control the channel multiplexing and receives the serial output from the resulting A/D conversions, converting the data from serial to parallel and storing the results in a memory block within the FPGA itself. The saved position locations of the faders are eight 10-bit registers located on word boundaries. These registers are cleared upon power-on or after a software reset.

Motor Power (12V) Sensing (sheet 5)

Channel 2 of A/D U31 receives a voltage proportional to the main +12V, scaled by 1/3 by the voltage divider formed by R120/R121. The voltage divider scales supply voltages from 0 to 15V to be within the 0-5V range of the A/D.

Since LARC2 can be powered from the 960L or from the optional Power Pack, 12 volts can vary. This provides software with a means to monitor the voltage for the motor drivers. The output waveform can then be adjusted accordingly.

The 12V-sense register is cleared upon power-on or after a software reset.

Fader Nulling

Automatic nulling of a fader is based on a software feedback loop. When it is time to move the faders, algorithms within the code calculate the difference between the desired target position and the current A/D position data and issue appropriate control waveforms to the motors, factoring in the measurement of the actual motor supply-voltage.

Fader Touch-sensing (sheet 6)

Each motorized fader is equipped with an electrically-conductive knob which connects to a terminal of the fader through a sliding track. This feature makes it possible to sense when a knob is touched by an operator.

When an operator touches the knob, the apparent capacitance at the terminal increases due to the added capacitance of the operators body. This additional capacitance is detected in a bridge circuit where the apparent capacitance of the touch track is compared with a reference capacitor.

The terminal from channel 1 (TOUCH1) is coupled to comparator U28 by capacitor C118 and current-limiting resistor R103. The dual diodes of D22 are normally back biased; D22 protects the touch circuitry by diverting high-voltage triboelectric charge (static) either to ground or into C120/C199, biased at 5V by R87. In normal operation, D22 and R103 can be ignored.

The other comparator input is connected to a discrete 33pF capacitor (C119), and both comparator inputs are driven through individual 39.2K resistors (R104,R105) by a bridge excitation waveform. The excitation is produced from TCH_CLK, a 3.3V, 125kHz squarewave, buffered by emitter-follower Q8. Relative to the period of the squarewave, the time constants of the bridge are long enough that the comparator inputs are quasi-triangular. The relative amplitudes of the triangles depend on the relative capacitances at the two inputs.

When the knob is not touched, its capacitance is smaller than 33pF and the corresponding triangle at U28-3 is larger than that developed at U28-2. At the positive peak of the triangle, the comparison will be positive, and the output of U28 will therefore be high. At that point, the high level is latched by the TCH_CLK squarewave into U35, which drives TCH_DET1 from its inverting output. In the untouched state, TCH_DET1 is constantly low.

When the knob is touched, the capacitance becomes greater than 33pF, and the result of the comparison is opposite at all instants of time. The latched value is therefore opposite, and in the touched state, TCH_DET1 is constantly high.

The operation of the touch-sense circuits for the other odd-numbered faders is identical. The even-numbered circuits operate similarly, but their excitation square wave is of the opposite phase. This helps ensure proper touch sensing in the case where multiple knobs are touched simultaneously.

The states of TCH_DET[8:1] can be read by software via tri-state buffer U24 and the FPGA.
4.6. Joystick (sheet 5)
Channels 0 and 1 of A/D converter U31 are used to digitize the position of the two-axis joystick connected to J7 and J8. As with the faders, the joystick is supplied with 5Vdc, to produce position-dependent X and Y dc voltages, which are digitized by the two channels.

Piezo Transducer (sheet 5)

A piezoelectric ceramic transducer disk is mounted flat on the pc board, under the Lexicon button. When the button is pressed, it not only makes contact with switch pattern SP47, it also produces flexure of the piezo element. The resulting voltage is peak-detected and amplified by U29 (LM358), then digitized by A/D U31. The amplitude of the piezoelectric voltage gives an indication of how hard the button was pressed, which software can determine from the profile of the digitized waveform.
4.8. Notes on A/D Operation
The A/D reference and the potentiometer excitation voltages are the same, so the digitized position information from the potentiometers is a ratiometric measurement, insensitive to the exact value of the 5V excitation. In contrast, the accuracy of both the +12V sense and the piezo transducer channels do depend on the accuracy of 5VA, which is +/5%.

The hardware-controlled interface implemented in the FPGA produces all the A/D control words, clock, and chip-selects. The serial bit clock rate is 2MHz. The entire A/D scan cycle takes 200usec, so each channel is

sampled 5000 times per second. The serial data is stored in parallel form in a memory block within the FPGA, where software can read it via the FPGA parallel port as necessary.

PS/2 Keyboard Interface (sheet 7)

The PS/2 port (J19) allows the user to connect a PS/2 compatible keyboard to LARC2. Clock and bidirectional data are driven by open-collector nand gate U1 (74ALS38) Logic within the FPGA receives incoming serial data from the keyboard, checks the parity, and presents the data to the system as a byte of data at address 0x1000 0700. The controller does not translate the scan codes. The controller also passes command information serially with parity appended to the auxiliary device through address 0x1000 0700. A read-only status register resides at 0x1000 0704.The PS/2 controller is a pass through interface and does not support any of the controller commands.

Input and Output Registers

The output buffer is an 8-bit read-only register at address 0x1000 0700. When the output buffer is read, the controller sends information to the SA-1100. The information can be keyboard scan codes or auxiliary device data.
The input buffer is an 8-bit write-only register at address 0x1000 0700. When the input buffer is written to, the input-buffer-full (bit 1) in the status byte is set to 1. The data is sent to the keyboard.
4.9.2. PS/2 Status Register
The PS/2 Status Register is an 8-bit read-only register at address 0x1000 0704.
4.9.3. Interrupts
The PS/2 Controller produces two interrupts TXRDY and RXRDY. TXRDY is connected to GPIO11 on the SA-1100 and indicates that the input buffer is empty. This bit is set to 1 on power-on or reset. RXRDY is connected to GPIO12 on the SA-1100 and indicates that that there is a byte in the output buffer. This is set to 0 on power-on or reset.

LCD Interface (sheet 7)

The LCD interface that is on the LARC2 is a Passive Matrix Color Display with 640 x 240 dots.
This display is driven directly from the LCD interface native to the SA-1100 microprocessor. Encoded pixel data is stored in the external DRAM and the LCD controller has its own dedicated DMA controller for moving the data to the output FIFO. LCD contrast is adjustable by R136 (CONTRAST) located on the rear panel. R136 is enabled by CONT_ON/ permanently asserted low. J1 and J3 support the pinouts of alternative LCD modules.

Host Interface Port (sheet 7)

The Host Interface uses Serial Port 1 of the SA-1100. This port is a combination synchronous data link controller (SDLC) and universal asynchronous receiver/transmitter (UART) serial controller. This port is configured as a UART and is identical to Serial port 3. This connects to an ALS180 RS422 driver/receiver (U2).

The pinout for the host interface is shown below.

Pin	**Description**
1	Ground
2	~RXD
3	TXD
4	Ground (SC)
5	Plus 12 Volts DC
6	Ground (RC)
7	RXD
8	~TXD
9	Ground

Table 4-1 Host interface pinout

Option Board Interface (sheet 4)

Connector J6 brings out signals to support an additional plug-in option board for additional I/O and memory.

PCMCIA Interface

The SA-1100 provides control signals to support a two-slot PCMCIA interface. Slot 1 is used for the on-board program Flash memory and slot 2 is used for the option board PCMCIA card slot.

Expansion Serial Interfaces

Serial Port 0

Serial port 0 is a universal serial bus (USB) device controller that supports three endpoints and can operate half-duplex at a baud rate of 12Mbps (slave only, not a host or hub controller). This port is connected to the option board connector for future expansion.

Serial Port 2

Serial port 2 is an infrared communications port (ICP). It operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. This port is connected to the option board connector for future expansion.

Debug Interface

The debug Interface available through the option board connector uses Serial Port 3 of the SA-1100. This port is a combination synchronous data link controller (SDLC) and universal asynchronous receiver/transmitter (UART) serial controller. For LARC2, it is configured as a UART.

Power Supply

Power Source (sheet 7)

The LARC2 operates from a source of 10 to 12VDC, which may either come from the host 960L via the 9-pin HOST connector J20 or from a dc source connected to the EXT. POWER jack J21. When connected to the regulated 12VDC supply in the 960L, the LARC2 voltage at J20 will be lower due to IR losses in the 9-pin cable, and this limits the length of cable that can successfully supply the operating current of 1-to-2 Amps. A plug in J21 opens the switching contacts A&B, which disconnects the +12HOST and substitutes the external supply. External power on the center pin of J20 (pin D) connects through FB3 and D4. D4 prevents damage due to a misconnected external power jack (AC or the wrong polarity of DC).

Main 12V (sheet 7)

The voltage at the cathode of D4 connects through PS1 to become the main dc supply, nominally +12V, reduced by the diode drop. PS1 is a 0.75 Amp self-resetting thermally activated fuse. Normally, the fuse exhibits a low series resistance, a few tenths of an ohm. When overloaded by currents >1.5Amp, the fuse undergoes self-heating and switches to a high resistance state due to the thermal characteristics of its material. This high resistance limits the current drawn from the supply under the overload condition. The fuse maintains the high-resistance state as long as it dissipates about 0.8W, or about 66mA at 12V, which is the short-circuit condition. The trip time is typically 0.2 seconds at 8 Amps, which is a severe overload. Smaller overloads can take many seconds to trip. Resetting occurs when the load is removed and the fuse cools, returning to the low-resistance state. When PS1 is tripped, the voltage across it is sufficient to supply current through R16 to illuminate LED D3. D3 glows as an indication that the fuse has tripped, visible through the ventilation slits in the bottom rear cover.

LCD Backlight (sheet 7)

The backlight built into the color LCD module is based on a Cold Cathode Fluorescent Lamp (CCFL), which requires high-voltage ac to operate. This voltage is generated by the inverter module mounted in the LCD display housing. The inverter is rated to produce an output of 900VACrms from for an input voltage of 5 to 12 VDC. Regulator U4 (LM2941) supplies this input voltage and protects the inverter by going into regulation if the input is too high due to misconnection. U4 is a low-dropout type and normally delivers nearly full voltage to the inverter, with only around 1/2 volt across the regulator itself.

On/off and brightness of the LCD backlight is determined by the control characteristics of the inverter module, from control lines connected along with the dc power via J2. Logic level LCD_VBR from the cpu switches transistor Q2 to set brightness control voltage VBR/ for two brightness levels, from 0Vdc (bright) to 1.6Vdc (dim). Logic level LCD_VRMT/ drives transistor Q1 to switch the on/off control VRMT between +5V (backlight on) and ground (backlight off).

Main 5V (sheet 9)

The main +5V logic supply is derived from +12V by switching regulator U40 (LM2676). The switching pulse waveform at pin 1 (SW) of U40 is filtered by L1 and C15 to produce +5Vdc, which is the average value of the pin-1 voltage. The positive excursion of the switching pulse is produced by the series switch within U40, which connects pin 1 (SW) to pin 2 (VIN), which is the main +12V heavily-decoupled by FB5 and associated capacitors. When the switch is off, the negative excursion of the switching pulse drops to a fraction of a volt below 0, determined by the forward voltage of catch diode D25. The switching frequency remains constant, at around 260 kHz. The regulator senses the filtered 5V fed back into pin 6 (FB) and varies the switching duty cycle to maintain regulation. The switching regulator efficiently converts the relatively high-voltage low-current 10-to-12V input into the low-voltage high-current 5V output. At lower input voltages, the regulator draws more current to provide the constant power consumed by the 5V output load.

3.3V and 2V (sheet 9)

The 3.3V logic supply is derived from the 5V by a fixed-voltage, linear regulator, U3 (LM3940). The 2V logic supply is derived from the 5V by adjustable linear regulator U7 (LM317), set to 2V by R34/R35.

Register Summary

The following is a full map of the physical address space (all addresses in hex):

Address	Symbol	Name
0000 0000 – 0001 FFFF		Boot flash
0800 0000 – 087F FFFF		Program flash (alternate)
1000 0000 – 1000 001C	MTRWFn	Motor waveform register
1000 0100	MTRENA	Motor enable register
1000 0102	MTRDIR	Motor direction register
1000 0104	MTSHR	Motor Shift Rate
1000 0200	ADCMD	A/D command register
1000 0300 – 1000 030E	SLDPOSn	Fader n position register
1000 0310	JOYSTKX	Joystick X-axis register
1000 0312	JOYSTKY	Joystick Y-axis register
1000 0314	P12VSEN	Plus 12 volt sense register
1000 0316	TAPDR	Tap data register
1000 0400	METER0	Meter bridge register0
1000 0402	METER1	Reserved for Meter bridge register1
1000 0404	KEYLED	Keypad LED Register
1000 0500 – 1000 05008	KEYDAT	Keypad data registers
1000 0600	TCHDAT	Touch data register
1000 0700	PS/2DDAT	PS/2 Data Register

1000 0702	PS/2STAT	PS/2 Status Register
1800 0000 – 1800 0002	CS3REG	CS3 Register
2000 0000 – 2000 FFFF		PCMCIA socket 1 I/O space
2800 0000 – 2800 FFFF		PCMCIA socket 1 attribute space
2C00 0000 – 2C00 FFFF		PCMCIA socket 1 memory space
3000 0000 – 3000 FFFF		PCMCIA socket 2 I/O space
3800 0000 – 3800 FFFF		PCMCIA socket 2 attribute space
3C00 0000 – 3C00 FFFF		PCMCIA socket 2 Memory space
8000 0000	UDCCR	UDC control register
8000 0004	UDCAR	UDC address register
8000 0008	UDCOMP	UDC OUT max packet register
8000 000C	UDCIMP	UDC IN max packet register
8000 0010	UDCCS0	UDC endpoint 0 cntl/status reg
8000 0014	UDCCS1	UDC endpoint 1 cntl/status register
8000 0018	UDCCS2	UDC endpoint2 cntl/status register
8000 001C	UDCD0	UDC endpoint 0 data register
8000 0020	UDCWC	UDC endpoint 0 write count register
8000 0028	UDCDR	UDC xmit/rec data register (fifo)
8001 0000	UT1CR0	UART 1 control register 0
8001 0004	UT1CR1	UART 1 control register 1
8001 0008	UT1CR2	UART 1 control register 2
8001 000C	UT1CR3	UART 1 control register 3
8001 0014	UT1DR	UART 1 data register
8001 001C	UT1SR0	UART 1 status register 0
8001 0020	UT1SR1	UART 1 status register 1
8002 0060	SDCR0	SDLC control register 0
8002 0064	SDCR1	SDLC control register 1
8002 0068	SDCR2	SDLC control register 2
8002 006C	SDCR3	SDLC control register 3
8002 0070	SDCR4	SDLC control register 4
8002 0078	SDDR	SDLC data register
8002 0080	SDSR0	SDLC status register 0
8002 0084	SDSR1	SDLC status register 1
8003 0000	UT2CR0	UART 2 control register 0
8003 0004	UT2CR1	UART 2 control register 1
8003 0008	UT2CR2	UART 2 control register 2
8003 000C	UT2CR3	UART 2 control register 3
8003 0010	UT2CR4	UART 2 control register 4
8003 0014	UT2DR	UART 2 data register
8003 001C	UT2SR0	UART 2 status register 0
8003 0020	UT2SR1	UART 2 status register 1
8004 0060	HSCR0	HSSP control register 0
8004 0064	HSCR1	HSSP control register 1

8004 006C	HSDR	HSSP data register
8004 0070	HSSR0	HSSP status register 0
8004 0078	HSSR1	HSSP status register 1
8005 0000	UT3CR0	UART 3 control register 0
8005 0004	UT3CR1	UART 3 control register 1
8005 0008	UT3CR2	UART 3 control register 2
8005 000C	UT3CR3	UART 3 control register 3
8005 0014	UT3DR	UART 3 data register
8005 001C	UT3SR0	UART 3 status register 0
8005 0020	UT3SR1	UART 3 status register 1
8006 0000	MCCR0	MCP control register 0
8006 0008	MCDR0	MCP data register 0
8006 000C	MCDR1	MCP data register 1
8006 0018	MCSR	MCP Status register
8007 0060	SSCR0	SSP control register 0
8007 0064	SSCR1	SSP control register 1
8007 006C	SSDR	SSP data register
8007 0074	SSSR	SSP status register
9000 0000	OSMR0	OS timer match register 0
9000 0004	OSMR1	OS timer match register 1
9000 0008	OSMR2	OS timer match register 2
9000 000C	OSMR3	OS timer match register 3
9000 0010	OSCR	OS timer counter register
9000 0014	OSSR	OS timer status register
9000 0018	OWER	OS timer watchdog enable register
9000 001C	OIER	OS timer interrupt enable register
9001 0000	RTCAR	Real-time clock alarm register
9001 0004	RTCNR	Real-time clock count register
9001 0008	RTCTR	Real-time clock trim register
9001 0010	RTCSR	Real-time clock status register
9002 0000	PMCR	Power manager control register
9002 0004	PSSR	Power manager sleep status register
9002 0008	PSPR	Power manager scratchpad register
9002 000C	PWER	Power manager wakeup enable register
9002 0010	PCFR	Power manager configuration register
9002 0014	PPCR	Power manager PLL configuration
9002 0018	PGSR	Power manager GPIO sleep state
9002 001C	POSR	Power manager oscillator status
9003 0000	RSRR	Reset controller software reset
9003 0004	RCSR	Reset controller status register
9003 0008	TUCR	Reserved for test
9004 0000	GPLR	GPIO pin level register

9004 0004	GPDR	GPIO pin direction register
9004 0008	GPSR	GPIO pin output set register
9004 000C	GPCR	GPIO pin output clear register
9004 0010	GRER	GPIO rising-edge register
9004 0014	GFER	GPIO falling-edge register
9004 0018	GEDR	GPIO edge detect status register
9004 001C	GAFR	GPIO alternate function register
9005 0000	ICIP	Interrupt controller IRQ pending
9005 0004	ICMR	Interrupt controller mask register
9005 0008	ICLR	Interrupt controller level register
9005 000C	ICCR	Interrupt controller control register
9005 0010	ICFP	Interrupt controller FIQ pending
9005 0020	ICPR	Interrupt controller pending register

Meter Bridge Module

The meter bridge circuitry is represented on schematic 060-13389. The module connects to the main board via J4 (main board sheet 7). The meter bridge consists of 24 LEDs in a three row by eight column matrix. The LEDs are divided into two groups, each controlled by an 8 bit register (U1, U2, sheet 1). Software writes a sequence of bit patterns to activate the groups one at a time turning on the LEDs in that group.

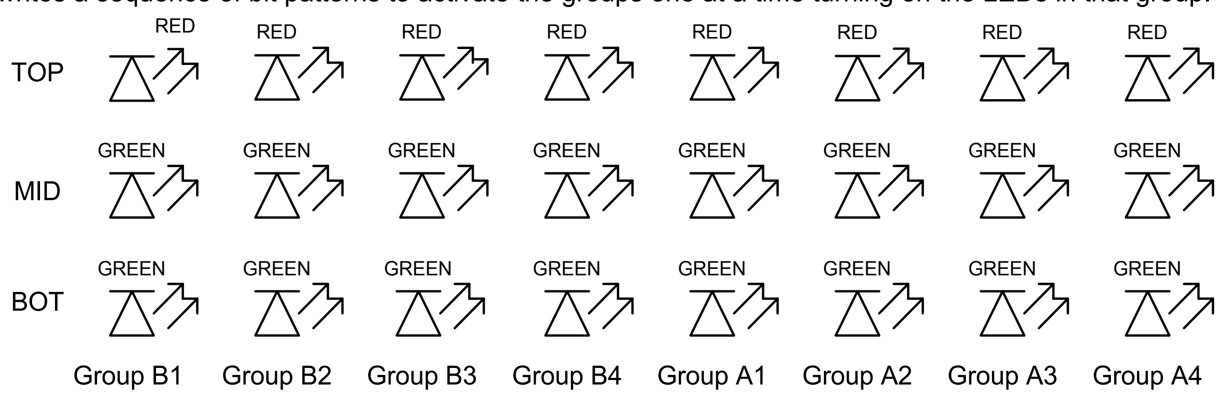


Figure 7-1 Meter Bridge

Chapter 8 - Parts List

CHASSIS/MECHANICAL

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
530-02488	TIE,CABLE,NYL,.14"X5 5/8"	8		
540-14303	GROMMET,STRIP,SER,.037"GAP,NYL	4		SUPPORT,CENTER
600-13984	CARD GUIDE,1/16PCB,4"L,3"MTG	10		
630-14304	WSHR,FL,.170IDX.375ODX.093,RUB	2		PWR SUP TO CHASSIS
630-14358	WSHR,FL,#6CLX1/4ODX1/16,NYL	1		STOP TO STOP SUPP
630-14514	WSHR,FL,#6CLX1/4ODX1/32,BLKNYL	2		FRONT PANEL
640-01711	SCRW,6-32X1/4,FH,PH,ZN	8		
640-01716	SCRW,6-32X3/8,PNH,PH,ZN	28		
640-02704	SCRW,6-32X1/4,PNH,PH,BLK	22		
640-03675	SCRW,6-32X1-1/4,PNH,PH,ZN	4		FAN ASSY
640-04339	SCRW,4-40X1/4,PNH,PH,SEMS,ZN	15		NLX BPL TO CTR SUPP
640-10498	SCRW,M3X6MM,PNH,PH,BZ	18		PS BRKT TO PS
640-13996	SCRW,10-32X1/2,FH,PH,BZ	6		
641-01703	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	3		RVB BD/MIDI BD MTG
641-13116	SCRW,TAP,AB,4X3/8,FH,PH,BZ	8		
643-01728	NUT,6-32,KEP,ZN	5		
643-08200	NUT,4-40,HEX,ZN	2		STOP BRKT TO FP
644-01735	WSHR,FL,#6CLX3/8ODX1/32THK	1		
680-13988	CABLE,RECP/DE9S,9C,18"L	1		NLX CPU (COM1) TO I/O BPL (J7)
680-13989	CABLE,RECP/DB15P,15C,18"L	1		MIDI BD TO I/O BPL (J8)
680-13990	CABLE,100,SCKT/SCKT,2X20C,2"L	2		I/O BPL (J11) TO NLX BPL (J14); I/O BPL (J10) TO NLX BPL (J15).
680-13991	CABLE,100,SCKT/SCKT,2X20C,6"L	1		
680-13992	CABLE,100,SCKT/SCKT,2X17C,6"L	1		FL DR TO NLX BPL (J7); PS CABLE TO FL DR
680-14203	CABLE,100,SCKT/SCKT,2X20C,9"L	1		HD DR TO NLX BPL (J9); PS CABLE TO HD DR
680-14206	CABLE,059,SCKT/SW&LED,4C,14"L	1		PWRSW TO NLXBPL(J20)
680-14305	CABLE,059,SCKT/SW,3C,14"L	1		RESET SW TO NLX BPL (J21)
680-14306	CABLE,100,SCKT/SCKT,2X5C,18"L	1		NLX CPU (COM2) TO I/O BPL (J6)
700-13965	RAIL,TOP/BOTTOM,960L	2		REAR OF CHASSIS
700-13967	COVER,TOP/BOTTOM,960L	2		
700-14406	FRAME,SUPP,AIR FILTER,4.46X3.6	1		
701-13346	BRACKET,NLX PS,960L	1		
701-13963	BRACKET,MTG,RACK,4U,960L	2		
701-13968	BRACKET,SUPPORT,FAN,960L	1		
701-13969	BRACKET,SUPPORT,CD/DISK,960L	4		
701-13985	PLATE,EXPANSION,BLANK,960L	1		
701-13986	PLATE,ACCESS,960L	1		
701-14308	BRACKET,SUPPORT,STOP,FP,960L	1		
701-14309	STOP,FP,960L	1		
702-13959	PANEL,FRONT,960L	1		
702-13972	PANEL,I/O,BLANK,960L	1		
702-13983	PLATE,MTG,HARD DRIVE,960L	1		
720-14404	GASKET,CONDFOAM,.2X.04X8.4,PSA	6		UNDER I/O PANELS

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
720-14405	AIR FILTER,4.3X3.5X.188,GRAY	1		
740-09538	LABEL,S/N,CHASSIS,PRINTED	1		CHASSIS, REAR
740-13573	LABEL,MFR ID,.9X.25,SILVER	1		
740-14348	LABEL,WINDOWS NT,960L	1		SIDE SUPPORT
750-13356	HD DRIVE,PROGRAMMED,960L	1		
750-13390	PWR SUP,+3.3V/+-5V/+-12V,300W	1		
750-13392	DRIVE,CD,IDE,32X,85MS,BLK	1		
750-13393	DRIVE,FLOPPY,3.5",1.44MB,BLK	1		
750-13950	CHASSIS,SUBASSY,960L	1		
750-14031	PCB ASSY,PCI,AUDIO,MIDI	1		TO NLX BPL (J4)
				NLX BPL BD ASSY
202-09794	RESSM,RO,0 OHM,0805	7		R1,4,7,10,104-106
202-09871	RESSM,RO,5%,1/10W,1K OHM	12		R98-103,154-158,164
202-09872	RESSM,RO,5%,1/10W,33 OHM	60		R13-42,52-81
202-09873	RESSM,RO,5%,1/10W,10K OHM	33		R2,3,5,6,8,9,11,12
				R94,113-120,122
				R126-140
202-10559	RESSM,RO,5%,1/10W,100 OHM	3		R107,109,111
202-10597	RESSM,RO,5%,1/10W,180 OHM	3		R108,110,112
202-10598	RESSM,RO,5%,1/10W,330 OHM	1		R162
202-12836	RESSM,RO,5%,1/10W,2.7K OHM2	3		R43-51,82-93,96,97
240-13216	CAPSM,ELEC,22uF,16V,20%	37		C3,5,8,9,11,13,20
				C22,25,27,29,33,35
				C37,39,43,45,47,54
				C56,59,68,71,73,76
				C78,80,84,86,88,90
				C94,96,98,101
				C103,106
245-09291	CAPSM,CER,470pF,50V,COG,5%	4		C120-122,124
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	63		C4,6,7,10,12,14-19
				C21,23,24,26,28
				C30-32,34,36,38
				C40-42,44,46,48-53
				C55,57,58,60,69,70
				C72,74,75,77,79
				C81-83,85,87,89
				C91-93,95,97,99,100
				C102,104,105,107
				C110,123
500-13944	CONN,EDGE,2X60C,.050,VERT,PCI	8		J1-4,10-13
500-13946	CONN,EDGE,2X170C,1MM,VERT,NLX	1		J6
510-01480	CONN,POST,156X045,HDR,3MCG,LOK	1		J22
510-13903	CONNSM,HDR,.059,6P,SHRD,POL	1		J20
510-13935	CONNSM,HDR,.059,3P,SHRD,POL	1		J21
510-13940	CONN,HDR,4.2MM,2X10C,POL,LATCH	1		J26
510-13941	CONN,POST,.100,HDR,2X17MCG,LP	1		J7
510-13942	CONN,POST,.100,HDR,2X20MCG,LP	4		J8,9,14,15

I/O BPL ASSY,960L

202-09794	RESSM,RO,0 OHM,0805	5		R1,42-45
202-09873	RESSM,RO,5%,1/10W,10K OHM	29		R4-15,17-33
202-10559	RESSM,RO,5%,1/10W,100 OHM	6		R2,16,34,36,38,40
202-10597	RESSM,RO,5%,1/10W,180 OHM	5		R3,35,37,39,41

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
240-12136	CAPSM,ELEC,33uF,10V,20%	5		C4,8,13,17,2O
240-13216	CAPSM,ELEC,22uF,16V,20%	5		C6,10,15,19,22
245-10416	CAPSM,CER,1000pF,50V,COG,5%	1		C1
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	12		C2,3,5,7,9,11,12,14 C16,18,21,23
330-10527	ICSM,DIGITAL,74HC138,SOIC	1		U1
500-13907	CONN,EURO,C,96P,abc,RECP,VERT	5		J1-5
510-13877	CONN,POST,.100,HDR,2X5MCG,LP	2		J6,7
510-13942	CONN,POST,.100,HDR,2X20MCG,LP	2		J10,11
510-13993	CONN,POST,.100,HDR,2X8MCG,LP	1		J8
510-13994	CONN,HDR,.200,4MC,SHRD	1		J9

I/O CLK BD ASSY,960L

202-09795	RESSM,RO,5%,1/10W,2.2K OHM	3		R19,22,25
202-09873	RESSM,RO,5%,1/10W,10K OHM	5		R2-4,27,30
202-09897	RESSM,RO,5%,1/10W,470 0HM	1		R5
202-09899	RESSM,RO,5%,1/10W,47 OHM	2		R1,16
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	5		R26,28,29,31,32
202-10558	RESSM,RO,5%,1/10W,47K OHM	3		R6,14,15
202-10559	RESSM,RO,5%,1/10W,100 OHM	1		R13
202-10947	RESSM,RO,5%,1/10W,680K OHM	1		R10
202-11072	RESSM,RO,5%,1/4W,220 0HM	5		R18,20,21,23,24
202-11073	RESSM,RO,5%,1/4W,270 OHM	1		R17
203-10424	RESSM,RO,1%,1/10W,4.99K OHM	4		R7-9,11
203-10895	RESSM,RO,1%,1/10W,681 OHM	1		R12
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	2		C13,16
240-10758	CAPSM,ELEC,1uF,50V,20%,5.5mmH	2		C8,20
240-13217	CAPSM,ELEC,47uF,16V,20%	2		C22,23
241-09798	CAPSM,TANT,10uF,10V,20%	1		C26
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	4		C9,12,14,17
245-09869	CAPSM,CER,.001uF,50V,Z5U,20%	2		C48,51
245-09895	CAPSM,CER,10pF,50V,COG,10%	1		C35
245-10561	CAPSM,CER,100pF,50V,COG,5%	4		C41-44
245-10562	CAPSM,CER,150pF,50V,COG,10%	4		C10,11,15,18
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	29		C1-7,19,21,24,25 C27-34,36-40,45-47 C49,50
270-00779	FERRITE,BEAD	2		FB13,16
270-06671	FERRITE CHOKE,2.5 TURN	2		FB3,4
270-11545	FERRITESM,CHIP,600 OHM,0805	0		FB1,2,5-12
270-12323	FERRITESM,CHIP,750 OHM,0805	4		FB14,15,17,18
270-14359	COILSM,VAR,1uH,5%,5.6X6.2X6MM	1		L1
300-10509	DIODESM,1N914,SOT23	2		D2,8
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	2		D9,10
300-10564	DIODESM,SCHOTTKY,LOW VF,SOT	2		D3,4
300-11599	DIODESM,GP,1N4002,MELF	2		D5,6
300-13881	DIODESM,VARACTOR,BB132	1		D7
310-10510	TRANSISTORSM,2N3904,SOT23	2		Q1,2
330-09796	ICSM,DIGITAL,74AC00,SOIC	1		U8
330-09889	ICSM,DIGITAL,74ACT04,SOIC	1		U12
330-10523	ICSM,DIGITAL,74HCU04,SOIC	1		U9
330-14355	ICSM,DIGITAL,74HC123A,SOIC	1		U5
330-14357	ICSM,DIGITAL,74FCTT/ABT244SOIC	1		U1
340-09244	ICSM,LINEAR,78LS05,5V REG,SOIC	1		U7

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
340-11573	ICSM,LIN,NJM4580,DUALOPAMP,SOP	1		U6
340-12111	ICSM,LIN,MC12148,VCO,LPWR,SOIC	1		U10
345-12038	ICSM,INTER,75ALS180,DR/RC,SOIC	3		U13-15
350-14373	ICSM,CPLD,960L,I/O CLK,V1.10	1		U2
375-12110	ICSM,OPTO-ISOL,HCPL0601,SOIC	1		U11
390-12978	CRYSTAL OSC,22.5792MHz,10PPM	1		U4
390-12979	CRYSTAL OSC,24.576MHz,10PPM	1		U3
430-10419	LEDSM,INNER LENS,RED	1		D1
440-13906	FUSESM,.75A,RESETTABLE,.18X.13	2		PS1,2
500-05855	CONN,EURO,C,ROW a+b+c,MALE,RA	1		J1
510-03550	CONN,DSUB,9FC,PCRA,4-40THD INS	2		J9,10
510-08634	CONN,BNC,1FC,MB,PCRA,GLD	1		J8
510-09790	CONN,DIN,5FC@180DEG,PCRA	3		J3-5
510-12326	CONN,BNC,PCRA,SELF-TERM,75	2		J6,7
527-12974	CONN,DSUB,JSCKT,4-40,.187X.25	4		DSUB(J9,10) TO PANEL
620-12915	LUG,SOLDER,.52IDX.7OD/FL.25TAB	2		J6,7
641-09699	SCRW,TAP,AB,#2X5/16,PNH,PH,ZN	3		DIN(J3-5) TO PANEL
643-04942	NUT,1/2-28,HEX,BRASS/NI	3		BNC(J6-8) TO PANEL
644-04943	WSHR,INT STAR,1/2"	3		BNC(J6-8) TO PANEL
702-13973	PANEL,I/O,CLK,960L	1		

AIN BD ASSY,960L

202-09794	RESSM,RO,0 OHM,0805	10		R1,10,17-24
202-09873	RESSM,RO,5%,1/10W,10K OHM	5		R7-9,11,16
202-09899	RESSM,RO,5%,1/10W,47 OHM	9		R2-6,12-15
202-10426	RESSM,RO,5%,1/10W,15K OHM	8		R81,84,85,88,89,92 R93,96
203-10583	RESSM,RO,1%,1/10W,10.0K OHM	16		R97-112
203-12363	RESSM,RO,1%,1/10W,90.9 OHM	16		R33-48
203-12477	RESSM,RO,1%,1/10W,13.3K OHM	8		R82,83,86,87,90,91 R94,95
203-13219	RESSM,THIN,1%,1/10W,422 OHM	8		R25-32
203-13917	RESSM,THIN,1%,1/10W,40.2K OHM	16		R113-128
203-13918	RESSM,THIN,.1%,1/10W,4.02K OHM	16		R49,52,53,56,57,60 R61,64,65,68,69,72 R73,76,77,80
203-14296	RESSM,THIN,1%,1/10W,6.49K OHM	16	02/17/00■	R161-176
203-14437	RESSM,THIN,.1%,1/10W,13.3K OHM	32		R129-160
203-14438	RESSM,THIN,.1%,1/10W,2.74K OHM	16		R50,51,54,55,58,59 R62,63,66,67,70,71 R74,75,78,79
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	2		C7,8
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	16		C83,85,87,89,91,93 C95,97,99,101,103 C105,107,109,111,113
240-11827	CAPSM,ELEC,10uF,16V,20%	24		C10,13,14,17,18,21 C22,25,50-58,61,62 C65,66,69,70,73
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	4		C2,3,5,6
245-10562	CAPSM,CER,150pF,50V,COG,10%	18		C1,4,82,84,86,88,90 C92,94,96,98,100,102 C104,106,108,110,112
245-11596	CAPSM,CER,6800pF,50V,COG,5%	8		C35,36,39,40,43,44 C47,48

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
245-11625	CAPSM,CER,33pF,50V,COG,5%	8		C59,60,63,64,67,68 C71,72
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	82		BC1A-H,BC2 BC8-27(+/-) C9,11,12,15,16,19,20 C23,24,26-34,37,38 C41,42,45,46,49 C74-81
270-06671	FERRITE CHOKE,2.5 TURN	2		FB1,2
270-09799	FERRITESM,CHIP,600 OHM,1206	8		FB3-10
270-11545	FERRITESM,CHIP,600 OHM,0805	16		FB11-26
300-11599	DIODESM,GP,1N4002,MELF	7		D1-5,7,8
340-11573	ICSM,LIN,NJM4580,DUALOPAMP,SOP	20		U8-27
340-11575	ICSM,LIN,7805,+5V REG,TO263	1		U3
350-13921	ICSM,FPGA,XCS05-3,10X10,PLCC	1		U1
350-14377	IC,SPROM,960L,AIN,V2	1		U2
355-13831	ICSM,ADC,AKM5393,24b,96kHz,SOP	4		U4-7
500-05855	CONN,EURO,C,ROW a+b+c,MALE,RA	1		J1
510-11086	CONN,XLR,3FC,PCRA,LATCH,SMALL	8		J2-9
520-00941	IC SCKT,8 PIN,LO-PRO,TIN	1		U2
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	16		XLR (J2-9) TO PANEL
702-13976	PANEL,I/O,AIN,960L	1		

AOUT BD ASSY,960L

202-09794	RESSM,RO,0 OHM,0805	1		R13
202-09795	RESSM,RO,5%,1/10W,2.2K OHM	6		R20,21,46,87,152,153
202-09873	RESSM,RO,5%,1/10W,10K OHM	5		R1-3,12,17
202-09899	RESSM,RO,5%,1/10W,47 OHM	6	■02/17/00	R7-11,14
202-09899	RESSM,RO,5%,1/10W,47 OHM	7	02/17/00■	R7-11,14,154
202-10946	RESSM,RO,5%,1/10W,3.3K OHM	5		R4-6,15,16
203-10896	RESSM,RO,1%,1/10W,1.00K OHM	1		R18
203-11697	RESSM,RO,1%,1/10W,909 OHM	16		R90,95,97,103,106 R111,113,119,122,127 R129,135,138,143,145 R151
203-11743	RESSM,RO,1%,1/10W,100K OHM	24		R23,24,26,27,29,30 R32,33,35,36,38,39 R41,42,44,45,48,53 R58,63,68,73,78,83
203-11890	RESSM,RO,1%,1/10W,232 OHM	1		R19
203-11980	RESSM,THIN,1%,1/10W,10.0K OHM	32		R47,49,51,52,54,56 R57,59,61,62,64,66 R67,69,71,72,74,76 R77,79,81,82,84,86 R88,102,104,118,120 R134,136,150
203-12370	RESSM,RO,1%,1/10W,280 OHM	16		R91,94,96,100,107 R110,112,116,123,126 R128,132,139,142 R144,148
203-12371	RESSM,THIN,1%,1/10W,2.74K OHM	8		R22,25,28,31,34,37 R40,43

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
203-12719	RESSM,THIN,1%,1/10W,2.00K OHM	16		R89,93,98,101,105 R109,114,117,121 R125,130,133,137 R141,146,149
203-14296	RESSM,THIN,1%,1/10W,6.49K OHM	16		R50,55,60,65,70,75 R80,85,92,99,108,115 R124,131,140,147
240-00608	CAP,ELEC,2.2uF,50V,RAD	2		C13,14
240-09367	CAPSM,ELEC,10uF,25V,NONPOL,20%	16		C165-180
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	5	■02/17/00	C11,12,18,21 C205 (across C28)
240-09786	CAP,ELEC,100uF,25V,RAD,LOW ESR	6	02/17/00■	C11,12,18,21,205,206
240-11111	CAPSM,ELEC,47uF,6V,NONPOL,20%	8		C157-164
240-12330	CAPSM,ELEC,2.2uF,35V,20%	8		C93,96,99,102,105 C108,111,114
240-13803	CAP,ELEC,560uF,35V,RAD,LOW ESR	1		C15
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	32		C29,31,33,35,37,39 C41,43,47,50,53,56 C59,62,65,68,70,71 C73,74,76,77,79,80 C82,83,85,86,88,89 C91,92
244-09390	CAP,MYL,.01uF,5%,RAD,MINI	8		C181,184,187,190 C193,196,199,202
244-10423	CAP,MYL,.22uF,50V,RAD,5%,BOX	4		C2,3,17,20
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	7		C22-28
245-10416	CAPSM,CER,1000pF,50V,COG,5%	16		C119,120,122,123,129 C130,132,133,139,140 C142,143,149,150 C152,153
245-10544	CAPSM,CER,220pF,50V,COG,5%	24		C94,95,97,98,100,101 C103,104,106,107,109 C110,112,113,115,116 C121,126,131,136,141 C146,151,156
245-10562	CAPSM,CER,150pF,50V,COG,10%	22		C1,4,7,8,16,19,182 C183,185,186,188,189 C191,192,194,195,197 C198,200,201,203,204
245-11593	CAPSM,CER,4700pF,50V,COG,5%	16		C117,118,124,125,127 C128,134,135,137,138 C144,145,147,148 C154,155
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	85		BC1A-H;BC2 BC14-33(+/-) C5,6,9,10,30,32,34 C36,38,40,42,44,45 C46,48,49,51,52,54 C55,57,58,60,61,63 C64,66,67,69,72,75 C78,81,84,87,90
270-00779	FERRITE,BEAD	16		FB37-52
270-06671	FERRITE CHOKE,2.5 TURN	4	■02/17/00	FB1-4
270-06671	FERRITE CHOKE,2.5 TURN	6	02/17/00■	FB1-4,53,54

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
270-09799	FERRITESM,CHIP,600 OHM,1206	16		FB5-20
270-11545	FERRITESM,CHIP,600 OHM,0805	16		FB21-36
300-10509	DIODESM,1N914,SOT23	2		D10,11
300-11599	DIODESM,GP,1N4002,MELF	13		D1-5,7-9,16,19-22
300-14286	DIODESM,SCHOTTKY,1A,SMB	6		D12-15,17,18
310-10422	TRANSISTORSM,2N4403,SOT23	1		Q2
310-10510	TRANSISTORSM,2N3904,SOT23	8		Q3,5,7,9,11,13,15,17
310-10565	TRANSISTORSM,2N3906,SOT23	8		Q4,6,8,10,12,14 Q16,18
310-10566	TRANSISTORSM,2N4401,SOT23	5		Q1,19-22
330-12143	ICSM,DIGITAL,74ACT244,SSOP	1		U5
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1		U4
340-11573	ICSM,LIN,NJM4580,DUALOPAMP,SOP	4		U22-25
340-11575	ICSM,LIN,7805,+5V REG,TO263	1		U3
340-12936	ICSM,LIN,OPA2134,DU OP AMP,SO8	8		U14-21
340-13911	ICSM,LIN,DRV134,BAL LINE DRVR	8		U26-33
350-13921	ICSM,FPGA,XCS05-3,10X10,PLCC	1		U1
350-14378	IC,SPROM,960L,AOUT,V1	1		U2
355-13987	ICSM,DAC,AD1853,24BIT,SSOP	8		U6-13
410-11639	RELAY,2P2T,DIP,5V,HI SENS	8		RY1-8
500-05855	CONN,EURO,C,ROW a+b+c,MALE,RA	1		J1
510-10881	CONN,XLR,3MC,PCRA,PLASTIC CMP	8		J2-9
520-00941	IC SCKT,8 PIN,LO-PRO,TIN	1		U2
620-12428	LUG,#4,INT STAR,XLR GND	8		J2-9
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	16		XLR (J2-9) TO PANEL
702-13978	PANEL,I/O,AOUT,960L	1		

AES BD ASSY,960L

202-09794	RESSM,RO,0 OHM,0805	29	■06/06/00	R1,36,37,39,40,42 R43,45,46,88-95;C48 C52,56,60;FB12-19
202-09794	RESSM,RO,0 OHM,0805	29	06/06/00■	R1,36,37,39,40,42 R43,45,46,88-95 R108-119
202-09871	RESSM,RO,5%,1/10W,1K OHM	2		R16,17
202-09873	RESSM,RO,5%,1/10W,10K OHM	8		R2,3,18,31-35
202-09897	RESSM,RO,5%,1/10W,470 0HM	4		R23,25,27,29
202-09899	RESSM,RO,5%,1/10W,47 OHM	16		R4-15,24,26,28,30
202-10890	RESSM,RO,5%,1/10W,220 OHM	1		R22
202-11496	RESSM,RO,0 OHM,1206	24		R48,50,52,54,56-71 R98,101,104,107
202-12365	RESSM,RO,5%,1/4W,110 OHM	4		R38,41,44,47
202-12366	RESSM,RO,5%,1/4W,22 OHM	16		R72-87
240-12136	CAPSM,ELEC,33uF,10V,20%	2		C1,2
241-09798	CAPSM,TANT,10uF,10V,20%	4		C17,20,23,26
244-11589	CAP,MYL,.068uF,63V,RAD,5%,BOX	4		C19,22,25,28
245-10562	CAPSM,CER,150pF,50V,COG,10%	4		C41-44
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	34		C3-16,18,21,24 C27,29-40,45,49 C53,57
270-11545	FERRITESM,CHIP,600 OHM,0805	4		FB4,6,8,10
270-13572	FERRITESM,CHIP,200 OHM,0805	7		FB1-3,5,7,9,11
270-14441	CHOKESM,COMMON,50V,2A,2LINE	4		L1-4
330-13866	ICSM,DIGITAL,74VHC244,SOIC	2		U4,5

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
330-13867	ICSM,DIGITAL,74VHC245,SOIC	1		U1
345-14245	ICSM,INTER,CS8403A,XMTR,SOIC	4		U10-13
345-14246	ICSM,INTER,CS8413,RCVR,SOIC	4		U6-9
350-14205	ICSM,FPGA,XCS10-3,14X14,VQFP	1		U2
350-14376	IC,SPROM,960L,AES,V2	1		U3
430-10421	LEDSM,INNER LENS,GRN	1		D1
470-12913	XFORMER,PULSE,AES,1:1,.2X.4SP	8		TX2,4,6,8,10,12 TX14,16
490-02356	CONN,JUMPER,.1X025,2FCG	4		W1-4 pins 2&3
500-05855	CONN,EURO,C,ROW a+b+c,MALE,RA	1		J1
510-02899	CONN,POST,100X025,HDR,3MC	4		W1-4
510-10881	CONN,XLR,3MC,PCRA,PLASTIC	4		J7-10
510-11086	CONN,XLR,3FC,PCRA,LATCH,SMALL	4		J3-6
520-00941	IC SCKT,8 PIN,LO-PRO,TIN	1		U3
620-12428	LUG,#4,INT STAR,XLR GND	4		J7-10
641-11466	SCRW,TAP,#4X3/8,PNH,PH,BZ,TRI	16		XLR (J3-10) TO PANEL
702-13980	PANEL,I/O,AES,960L	1		

RVB BD ASSY,960L

202-09794	RESSM,RO,0 OHM,0805	1		R169
202-09871	RESSM,RO,5%,1/10W,1K OHM	22		R41,42,52-56,63,116 R122,125,133,141-143 R161-164,191,195,196
202-09873	RESSM,RO,5%,1/10W,10K OHM	110		R12-39,43-51,57,58 R65-69,71-80,83-87 R89-92,94-102 R105-112,118-121 R123,124,126,140 R145,146,159,160 R166-168,172,173 R177,180-182,184 R186-190,192-194
202-09899	RESSM,RO,5%,1/10W,47 OHM	34		R59-62,113-115 R117,127-132,134-139 R144,147-158,183
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	9		R40,170,171,174-176 R178,179,185
202-10559	RESSM,RO,5%,1/10W,100 OHM	4		R70,82,93,104
202-10569	RESSM,RO,5%,1/10W,10 OHM	4		R64,81,88,103
202-10947	RESSM,RO,5%,1/10W,680K OHM	1		R165
202-10948	RESSM,RO,5%,1/10W,390 OHM	1		R9
202-11073	RESSM,RO,5%,1/4W,270 OHM	8		R1-8
203-10575	RESSM,RO,1%,1/10W,523 OHM	1		R11
203-11077	RESSM,RO,1%,1/10W,237 OHM	1		R10
240-11827	CAPSM,ELEC,10uF,16V,20%	5		C19,22,23,26,27
240-12136	CAPSM,ELEC,33uF,10V,20%	7		C3,5,6,9,10,21,29
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	4		C34,45,56,67
245-10976	CAPSM,CER,47pF,50V,COG,5%	2		C114,115
245-12460	CAPSM,CER,.056uF,50V,X7R,20%	1		C122
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	133		C1,2,4,7,8,11-18,20 C24,25,28,30-33 C35-44,46-55,57-66 C68-113,116-121 C123-152

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
300-11599	DIODESM,GP,1N4002,MELF	2		D9,10
330-09893	ICSM,DIGITAL,74ACT157,SOIC	1		U45
330-11990	ICSM,LEXICHIP3B,100PIN,PQFP	4		U40,42,46,48
330-12321	ICSM,DIGITAL,74VHCT08,TSSOP	1		U38
330-12461	ICSM,DIGITAL,74FCT2244AT,QSOP	15		U1,U3-9,13,14,30-32 U44,50
330-14247	ICSM,DIGITAL,74VHCT245,SOIC	1		U39
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1		U2
340-12119	ICSM,LIN,TL7705,+5V MON,SOIC	1		U37
346-12072	ICSM,SS SWITCH,QS3245,QSOP	3		U10-12
350-12637	ICSM,DRAM,1MX16,70NS,SOJ	4		U41,43,47,49
350-14248	ICSM,SRAM,128KX8,70NS,SOIC	2		U28,29
350-14287	ICSM,SRAM,2PORT,2KX8,55NS,PLCC	2		U25,27
350-14364	ICSM,ROM,27256,960L,RVB,V1.00	1		U18
350-14365	ICSM,GAL,16V8,960L,TMXSEL,V100	1		U16
350-14366	ICSM,GAL,16V8,960L,56KDEC,V100	1		U17
350-14367	ICSM,GAL,16V8,960L,56KSTB,V100	1		U19
350-14368	ICSM,GAL,16V8,960L,LXCTL,V100	1		U20
350-14369	ICSM,GAL,16V8,960L,LXSTB,V100	1		U23
350-14370	ICSM,GAL,16V8,960L,ZLXIF,V100	1		U26
350-14371	ICSM,GAL,16V8,960L,ZLXCLK,V100	1		U35
365-09883	ICSM,uPROC,Z80,CMOS,10MHz,QFP	2		U33,36
365-12047	ICSM,uPROC,TMIX,144PIN,TQFP	3		U21,22,24
365-12315	ICSM,uPROC,DSP,56301,80MHz,TQF	1		U15
390-12075	CRYSTALSM,6MHz,PAR,18pF	1		Y1
390-12427	CRYSTAL OSCSM,50MHz	1		U34
430-10421	LEDSM,INNER LENS,GRN	8		D1-8
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	4		BRKTS TO RVB BD(2EA)
701-13970	BRACKET,PCI BD,LEFT,960L	1		
701-13971	BRACKET,PCI BD,RIGHT,960L	1		

NLX CPU BD ASSY

640-02704	SCRW,6-32X1/4,PNH,PH,BLK	2		NLX CPU TO BRKT
701-14307	BRACKET,SUPPORT,NLX CPU,960L	1		
701-14311	SHIELD,I/O,NLX CPU,~9.3X1.9"H	1		RETAINER CLIPS TO PCB--2PLCS
750-14030	PCB ASSY,NLX CPU,2DIMM,10X8.25	1		
750-14032	MODULE,SDRAM,32MB,100MHz,	1		
750-14033	CPU KIT,CELERON,300MHz,FAN HS	1		PLUG IN FAN CONN TO J1

NLX BPL EXT BD ASSY,960L

500-13944	CONN,EDGE,2X60C,.050,VERT,PCI	2		J20,21
510-13336	CONN,POST,.100,HDR,2X32P,LK,RA	2		J1,2
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	6		BRACKET MTG
701-13970	BRACKET,PCI BD,LEFT,960L	1		
701-13971	BRACKET,PCI BD,RIGHT,960L	1		

I/O BPL EXT BD ASSY,960L

500-05855	CONN,EURO,C,ROW a+b+c,MALE,RA	1		J1
500-14427	CONN,EURO,R,96P,abc,RECP,RA	1		J15
510-13336	CONN,POST,.100,HDR,2X32P,LK,RA	2		J12,13

LARC2:

CHASSIS/MECHANICAL:

MAIN HSG ASSY,LARC2

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
120-14515	ADHESIVE,GLUE,HOT MELT,GP	1.135		CLIP TO FERRITE HOLDER
270-14401	FERRITE,FLAT CABLE,~.8X1.2,HW	1		INVERTER & DISPLAY CABLE
453-14226	KEYPAD,MAIN,LARC2	1		
453-14228	KEYPAD,SIDE,LARC2	1		
530-02489	TIE,CABLE,NYL,.1"X4"	1		
550-14035	KNOB,SLIDE,TANG,SATIN/BLK LN	8		
550-14230	KNOB,JOYSTICK,LARC2	1		
630-12533	WSHR,FL,.120IDX.25ODX.062,RUB	4		
640-01716	SCRW,6-32X3/8,PNH,PH,ZN	6		DSPLY HSG TO MN HSG
641-01715	SCRW,TAP,AB,6X3/8,PNH,PH,ZN	8		MAIN BD TO TOP
644-06347	WSHR,FL,.195IDX.437ODX.030THK	2		DSPLY HSG TO MAIN HSG--ON INSIDE OF UPPER MAIN HSG.
700-14208	HOUSING,TOP,LARC2	1		
700-14211	HOUSING,BOTTOM,LARC2	1		
701-14447	CLIP,.78LX.28WX.26H,.100/.156	1	■04/27/00	FERRITE MTG
701-14517	CLIP,.78LX.28WX.29H,.100/.156	1	04/27/00■	FERRITE MTG
720-14223	PAD,FOOT,LARC2	2		HSG, BOTTOM
740-09538	LABEL,S/N,CHASSIS,PRINTED	1		REAR PANEL
740-13573	LABEL,MFR ID,.9X.25,SILVER	1		REAR PANEL
740-14200	LABEL,WARN/APP,PRO,5.75X.98"	1		HSG, BOTTOM
740-14349	LABEL,WINDOWS CE,LARC2	1		MAIN BD (U8)

JOYSTICK ASSY,LARC2

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
200-13939	POT,STICK CTLR,10K,38MM SQ	1		
641-01703	SCRW,TAP,AB,4X1/4,PNH,PH,ZN	4		BRACKET TO POT
680-14239	CABLE,059,SCKT/ST&T,3C,3.5"L	2		
701-14215	BRACKET,JOYSTICK,LARC2	1		
720-07297	TAPE,COPPER,1/2"W	1		

DSPLY HSG ASSY,LARC2

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
380-13931	DC-AC INV,2W OUT,W/DIMMING	1		
640-01716	SCRW,6-32X3/8,PNH,PH,ZN	4		HSG REAR TO FRONT
640-14037	SCRW,0-80X1/4,PNH,PH,ZN	2		INVERTER TO METER BD
641-01715	SCRW,TAP,AB,6X3/8,PNH,PH,ZN	4		LCDBRKT TO DSPLY HSG
680-14235	CABLE,FFC,20CX.5MM,7.5"	1		TO METER BD (J1)
680-14238	CABLE,HSG/HSG,5C/6C,8.5"	1		TO INVERTER
700-14212	HOUSING,DSPLY,FRONT,LARC2	1		
700-14213	HOUSING,DSPLY,REAR,LARC2	1		
701-14447	CLIP,.78LX.28WX.26H,.100/.156	2		
703-14207	LENS,LCD,LARC2	1		
703-14221	OVLY,METER BRIDGE,LARC2	1		
720-14520	SPCR,PVC,~6.8X3.0X.02",BLK,ADH	1	07/26/00■	

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE

DISPLAY,LARC2 (SHARP or KYOCERA)

SHARP:

430-13934	DISP,LCD,640X240DOTS,COLOR	1		
680-14236	CABLE,FFC,20CX.5MM,12.5",FOLD	1		LCD TO MAIN BD (J1)
680-14240	CABLE,CONN/HSG,2C,2.5"	1		
701-14216	BRACKET,LCD,SHARP,LARC2	1		
720-10158	TAPE,FOAM,DBL-STK,.5WX.025THK	2		FFC CABLES TO BRKT (2).5" PC, (1)1" PC
720-14224	GASKET,LCD,SHARP,LARC2	1		

KYOCERA:

430-14034	DISP,LCD,640X240DOTS,COLOR,	1		CABLE TO METER BD
680-14237	CABLE,FFC,18CX.5MM,5.7",FOLD	1		
701-14217	BRACKET,LCD,KYOCERA,LARC2	1		CONN TO INVERTER
720-10158	TAPE,FOAM,DBL-STK,.5WX.025THK	1.5		FFC CABLES TO BRKT
720-14225	GASKET,LCD,KYOCERA,LARC2	1		

MAIN BD SUBASSY,LARC2

120-02023	ADHESIVE,SILICONE,RTV,CLEAR	0.050	06/14/00■	C14,15
120-09619	ADHESIVE,EPOXY,5-MIN	0.042		XDUCER
200-13938	POT,SLD,MOTOR,10K,60MMTRAV,	8		R139-146
200-14153	POT,RTY,10KB,KNURL,6MMX15MML	1		R136
202-09794	RESSM,RO,0 OHM,0805	5		R3,45,129,132; W1
202-09871	RESSM,RO,5%,1/10W,1K OHM	30		R11,13-15,19,31-33 R36,44,62,63,70,71 R74,77-80,106-113 R128,131,137
202-09872	RESSM,RO,5%,1/10W,33 OHM	5		R51-55
202-09873	RESSM,RO,5%,1/10W,10K OHM	37		R1,10,12,20,21,37,38 R42,43,47-50,57-61 R64-69,72,73,75,76 R83,84,90,91,96,97 R102,103,138
202-09874	RESSM,RO,5%,1/10W,2.2M OHM	1		R114
202-09899	RESSM,RO,5%,1/10W,47 OHM	2		R4,5
202-10557	RESSM,RO,5%,1/10W,4.7K OHM	5		R6-9,18
202-10559	RESSM,RO,5%,1/10W,100 OHM	1		R119
202-10571	RESSM,RO,5%,1/10W,100K OHM	1		R87
202-10586	RESSM,RO,5%,1/4W,100 OHM	7		R22-25,40,41,56
202-10597	RESSM,RO,5%,1/10W,180 OHM	1		R39
202-10836	RESSM,RO,5%,1/4W,1K OHM	1		R16
202-10892	RESSM,RO,5%,1/10W,2K OHM	12		R115,117,122-127 R130,133-135
202-11041	RESSM,RO,5%,1/10W,680 OHM	4		R17,27-29
202-13904	RESSM,RO,5%,1/10W,220K OHM	1		R116
203-10894	RESSM,RO,1%,1/10W,340 OHM	1		R120
203-10895	RESSM,RO,1%,1/10W,681 OHM	1		R121
203-11077	RESSM,RO,1%,1/10W,237 OHM	1		R34
203-12841	RESSM,RO,1%,1/10W,39.2K OHM	16		R81,82,85,86,88,89 R92-95,98-101 R104,105

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
203-12895	RESSM,RO,1%,1/10W,143 OHM	1		R35
240-11827	CAPSM,ELEC,10uF,16V,20%	1		C8
240-12136	CAPSM,ELEC,33uF,10V,20%	2		C6,17
240-13216	CAPSM,ELEC,22uF,16V,20%	1		C10
240-13217	CAPSM,ELEC,47uF,16V,20%	1		C99
240-13803	CAP,ELEC,560uF,35V,RAD,LOW ESR	2		C14,15
240-13913	CAPSM,ELEC,470uF,16V,20%	4		C141,143,145,147
241-09366	CAPSM,TANT,10uF,25V,20%	4		C90,92,150,153
241-11799	CAPSM,TANT,4.7uF,6.3V,20%	1		C39
245-09869	CAPSM,CER,.001uF,50V,Z5U,20%	3		C5,9,62
245-09875	CAPSM,CER,.1uF,50V,Z5U,20%	8		C91,98,100,106,107 C113,114,120
245-09876	CAPSM,CER,.01uF,50V,Z5U,20%	5		C11,18,27,29,152
245-10544	CAPSM,CER,220pF,50V,COG,5%	8		C93,96,101,104 C108,111,115,118
245-10976	CAPSM,CER,47pF,50V,COG,5%	2		C1,2
245-11625	CAPSM,CER,33pF,50V,COG,5%	12		C34,35,37,38,94,97 C102,105,109,112 C116,119
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	99		C3,4,7,12,13,16 C19-26,28,30-33,36 C40-61,63-89,95 C103,110,117 C121-140,142,144 C146,148,149,151
270-00779	FERRITE,BEAD	2		FB3,10
270-06671	FERRITE CHOKE,2.5 TURN	2		FB5,6
270-09799	FERRITESM,CHIP,600 OHM,1206	4		FB4,7-9
270-12323	FERRITESM,CHIP,750 OHM,0805	2		FB1,2
270-13802	INDUCTORSM,24uH,20%,2.74A	1		L1
270-13927	FERRITESM,CHIP,"T",EMI,1000pF	1		U9
300-10509	DIODESM,1N914,SOT23	7		D9-13,23,24
300-10563	DIODESM,DUAL,SERIES,GP,SOT23	10		D1,2,15-22
300-11599	DIODESM,GP,1N4002,MELF	3		D4,7,8
300-14286	DIODESM,SCHOTTKY,1A,SMB	1		D25
310-10422	TRANSISTORSM,2N4403,SOT23	4		Q4-6,9
310-10566	TRANSISTORSM,2N4401,SOT23	4		Q1,2,7,8
330-10535	ICSM,DIGITAL,74AC273,SOIC	1		U6
330-12073	ICSM,DIGITAL,74ALS38,SOIC	1		U1
330-13905	ICSM,DIGITAL,74LVC16244,TSSOP	1		U24
330-13924	ICSM,DIGITAL,74LVC16245A,TSSOP	1		U23
330-13925	ICSM,DIGITAL,74LVC162244,TSSOP	4		U15,19,21,22
330-14372	ICSM,DIGITAL,74HCT74,SOIC	4		U32-35
340-11045	ICSM,LIN,LM393,DUAL COMP,SOIC	4		U25-28
340-11559	ICSM,LIN,LM317M,+ADJ REG,DPAK	1		U7
340-11631	ICSM,LIN,LM358,DUAL OPAMP,SOIC	1		U29
340-12062	ICSM,LIN,LM3940,5-3V REG,TO263	1		U3
340-13806	ICSM,LIN,LM2676,5V REG,TO263	1		U40
340-13912	ICSM,LIN,ECONORESET,3.3,SOT223	1		U5
340-13926	ICSM,LIN,L293,4CH DRVR,SOIC	4		U36-39
340-14356	ICSM,LIN,LM2941C,ADJ,TO263	1		U4
345-12038	ICSM,INTER,75ALS180,DR/RC,SOIC	1		U2
350-13910	ICSM,DRAM,4MX16,60NS,TSOP	2		U11,17
350-13928	ICSM,FPGA,XCS10XL-4,14X14,TQFP	1		U18
350-13949	ICSM,FLASH,2MX8,3V,90NS,TSOP	4		U10,13,14,16

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
350-14374	IC,SPROM,LARC2,MAIN,V1.00	1		U41
350-14375	ICSM,FLASH,1M,LARC2,BOOT,V1.00	1		U12
355-13929	ICSM,ADC,TLV1548C,SAR,10b,SSOP	2		U30,31
365-13930	ICSM,uPROC,SA-1100,160MHz,TQFP	1		U8
390-12733	CRYSTAL OSCSM,2MHz,TRI	1		U20
390-13932	CRYSTALSM,32.768kHz,PAR	1		Y1
390-13933	CRYSTALSM,3.6864MHz,PAR,HC49	1		Y2
430-10419	LEDSM,INNER LENS,RED	1		D3
430-10421	LEDSM,INNER LENS,GRN	3		D5,6,14
430-13914	LEDSM,RED,100MCD,3.2X2.8MM	12		D26-31,34-39
440-13906	FUSESM,.75A,RESETTABLE,.18X.13	1		PS1
453-13916	SW,PBM,1P1T,7MMSQ,160GF,PCRA	1		SW1
480-13915	XDUCER,PIEZO-CER,2kHz,50MM LD	1		TO J9,10
500-13908	CONN,EURO,R,96P,abc,PLUG,VERT	1		J6
510-03484	CONN,DC POWER,PC,SMK S-G9314	1		J21
510-13902	CONNSM,FFC,.5MM,18POS,PCRA	1		J3
510-13903	CONNSM,HDR,.059,6P,SHRD,POL	1		J2
510-13909	CONN,MINIDIN,6FC,PCRA,SHLD,GND	1		J19
510-13935	CONNSM,HDR,.059,3P,SHRD,POL	10		J7,8,11-18
510-13936	CONNSM,FFC,.5MM,20POS,PCRA	2		J1,4
510-14172	CONN,DSUB,9MC,PCRA,4-40SCRW	1		J20
520-00941	IC SCKT,8 PIN,LO-PRO,TIN	1		U41
520-13901	IC SCKTSM,PLCC,44 PIN,W/O LOC	1	■07/24/00	U12
530-12360	STRAIN RELIEF,CABLE,MSA XFRMR	1		REAR PANEL
640-01701	SCRW,4-40X1/4,PNH,PH,ZN	5		FADER BRKT MTG (3); KEYSTONE TO PCB (2)
640-02812	SCRW,4-40X3/8,PNH,PH,BLK	3		RP TO KEYSTONES (2); STRAIN RELIEF (1)
640-14038	SCRW,M3X4MM,FH,SLOT,ZN,SMHD	16		BRACKET TO FADERS
680-14241	CABLE,059,SCKT/ST&T,3C,3/1.4"L	8		SOLDER GRN/YEL/BLK WIRES TO FADERS BEFORE ASSY TO BRKT
701-09640	BRACKET,KEYSTONE,621,4-40X2	2		PCB TO REAR PANEL
701-14214	BRACKET,FADER,LARC2	1		
702-14218	PANEL,REAR,LARC2	1		

METER BD ASSY,LARC2

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
202-09871	RESSM,RO,5%,1/10W,1K OHM	8		R1,6,7,11,12,16 R21,22
202-10586	RESSM,RO,5%,1/4W,100 OHM	6		R8-10,13-15
202-11041	RESSM,RO,5%,1/10W,680 OHM	8		R2-5,17-20
241-09798	CAPSM,TANT,10uF,10V,20%	2		C1,3
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	2		C2,4
310-10422	TRANSISTORSM,2N4403,SOT23	8		Q1-8
330-10535	ICSM,DIGITAL,74AC273,SOIC	2		U1,2
430-13900	LEDSM,GRN,25MCD,3.2X2.8MM	8		D3,6,9,12,15,18 D21,24
430-14312	LEDSM,RED,25MCD,3.2X2.8MM	8		D1,4,7,10,13,16 D19,22
430-14313	LEDSM,YEL,15MCD,3.2X2.8MM	8		D2,5,8,11,14,17 D20,23
510-13936	CONNSM,FFC,.5MM,20POS,PCRA	1		J1
635-14036	SPCR,SWAGE,0-80X1/4,1/8RD,ZN	2		INVERTER

OPT BD ASSY,LARC2

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
202-09873	RESSM,RO,5%,1/10W,10K OHM	9		R10-18
202-10559	RESSM,RO,5%,1/10W,100 OHM	3		R1-3
202-10586	RESSM,RO,5%,1/4W,100 OHM	1		R9
240-11827	CAPSM,ELEC,10uF,16V,20%	4		C26,28,30,32
245-12485	CAPSM,CER,.1uF,25V,Z5U,20%	17		C1-10,13,14,19,25 C27,29,31
330-13923	ICSM,DIGITAL,74LVC32A,TSSOP	1		U5
330-14314	ICSM,DIGITAL,74LVC125A,SOIC	1		U7
345-13140	ICSM,INTER,RS232 XCVR,+5V,SOIC	2		U1,2
350-14046	ICSM,GAL,22V10,LARC2,OPT,V1.00	1		U4
500-05930	CONN,EURO,C,ROW a+b+c,FEM,RA	1		J4
500-13907	CONN,EURO,C,96P,abc,RECP,VERT	1		J3
510-09773	CONN,MEM CARD,PC,68PIN	1		J2
510-09985	CONN,MEM CARD,68 PIN,EJECTOR	1		
510-14172	CONN,DSUB,9MC,PCRA,4-40SCRW	1		J1
640-01706	SCRW,4-40X3/8,PNH,PH,ZN	4		PCMCIA SCKT MTG
643-01733	NUT,4-40,HEX,SMALL,ZN	4		PCMCIA SCKT MTG

SHIP MAT'L/PACKAGING/MISCELLANEOUS

270-14402	FERRITE,RND CABLE,~.8X1.6,SNAP	1	50' CABLE
680-03525	CABLE,50',LARC	1	
730-04346	CARD,WARRANTY,LEXICON,8.5X11	1	
730-09509	CARD,REGISTRATION,GENERAL	1	
730-14316	CERTIFICATE,CE,960L/LARC2	1	
730-14317	BOX,17-1/2X12-3/4X9,LARC2	1	
730-14326	INSERT,FOAM,LARC2,LEFT	1	
730-14327	INSERT,FOAM,LARC2,RIGHT	1	
730-14347	CERTIFICATE,CE SA1100 DR,LARC2	1	
740-07693	LABEL,LEXICON DIG AUDIO,3"X5"	2	

POWER CORDS

680-09149	CORD,POWER,IEC,10A,2M,NA,SVT	1
680-08830	CORD,POWER,IEC,6A,2M,EURO	1
680-10093	CORD,POWER,IEC,5A,2M,UK	1
680-10096	CORD,POWER,IEC,6A,2M,AUSTRALIA	1
680-10097	CORD,POWER,IEC,6A,2M,JAPAN	1
680-10094	CORD,POWER,IEC,6A,2M,ITALY	1
680-10095	CORD,POWER,IEC,6A,2M,SWISS	1
680-10098	CORD,POWER,IEC,6A,2M,UNIVERSAL	1

SHIP MAT'L/PACKAGING/MISCELLANEOUS

070-14353	MANUAL,OWNER'S,960L	1
070-14354	NOTICE,S/W RELEASE,960L	1
541-00780	BUMPER,FEET,3-M #SJ5023	4
730-04346	CARD,WARRANTY,LEXICON,8.5X11	1
730-09509	CARD,REGISTRATION,GENERAL	1
730-14316	CERTIFICATE,CE,960L/LARC2	1
730-14350	BOX,24X22-3/4X11-1/2,LEXICON	1
730-14352	INSERT,FOAM,4UX17.5	2
730-14516	LICENSE AGREEMENT,END USER	1
740-07693	LABEL,LEXICON DIG AUDIO,3"X5	2
750-14300	CD,960L,V1.05	1

Spare Assemblies

PART NO.	DESCRIPTION	QTY	EFF■INACT	REFERENCE
021-14500	PL,SHIP,NLX BPL,TESTED,960L			
021-14501	PL,SHIP,I/O BPL,TESTED,960L			
021-14502	PL,SHIP,I/O CLK BD,TESTED,960L			
021-14503	PL,SHIP,AIN BD,TESTED,960L			
021-14504	PL,SHIP,AOUT BD,TESTED,960L			
021-14505	PL,SHIP,AES BD,TESTED,960L			
021-14506	PL,SHIP,RVB BD,TESTED,960L			
021-14507	PL,SHIP,NLX CPU BD,TESTED,960L			
021-14508	PL,SHIP,NLX EXT BD,TESTED,960L			
021-14509	PL,SHIP,I/O EXT BD,TESTED,960L			

Chapter 9 Schematics and Drawings

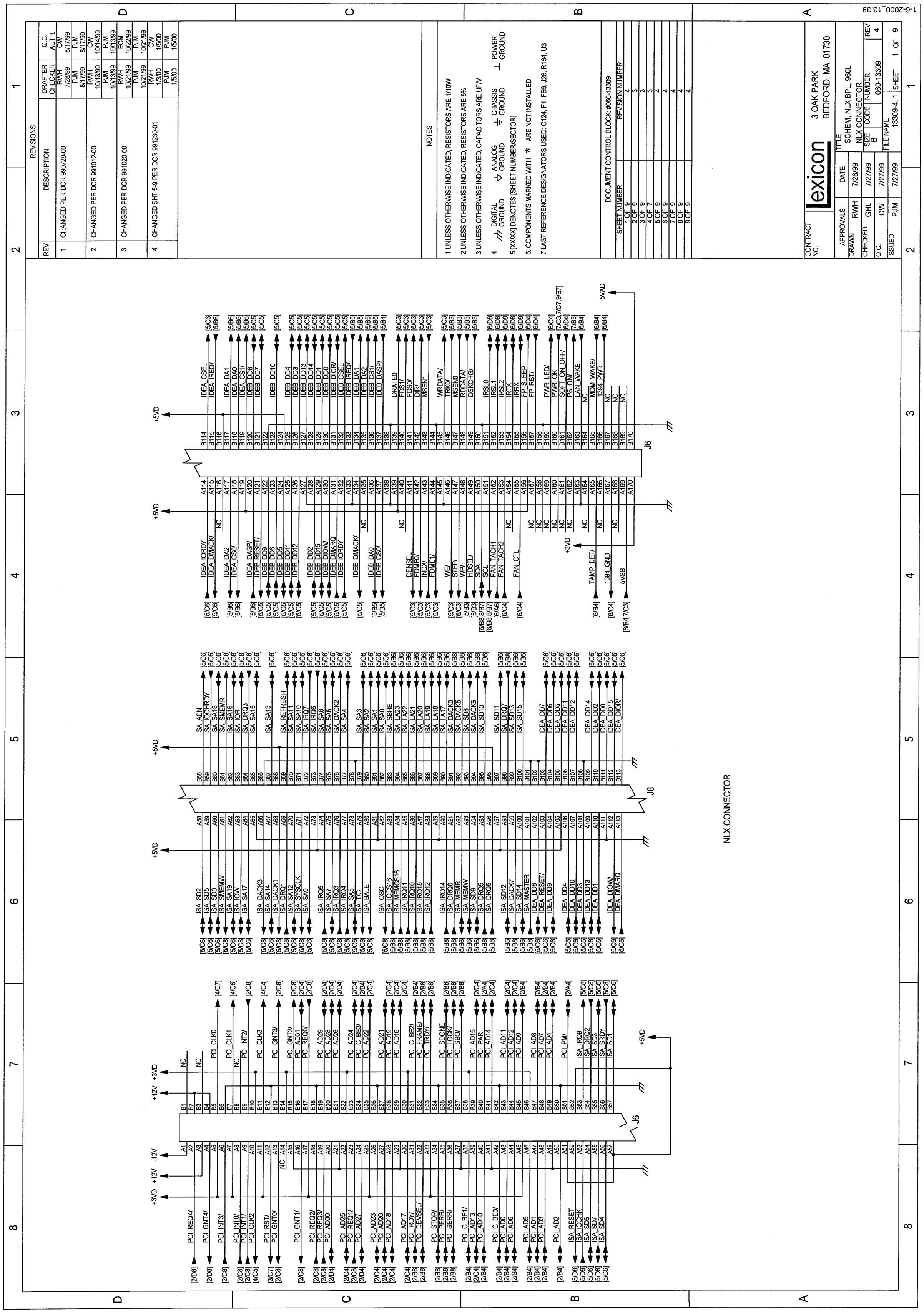
Schematics:

060-13309 SCHEM,NLX BPL,960L
060-13319 SCHEM,I/O BPL,960L
060-13329 SCHEM,I/O CLK BD,960L
060-13339 SCHEM,AIN BD,960L
060-13349 SCHEM,AOUT BD,960L
060-13359 SCHEM,AES BD,960L
060-13369 SCHEM,RVB BD,960L
060-13379 SCHEM,MAIN BD,LARC2
060-13389 SCHEM,METER BD,LARC2

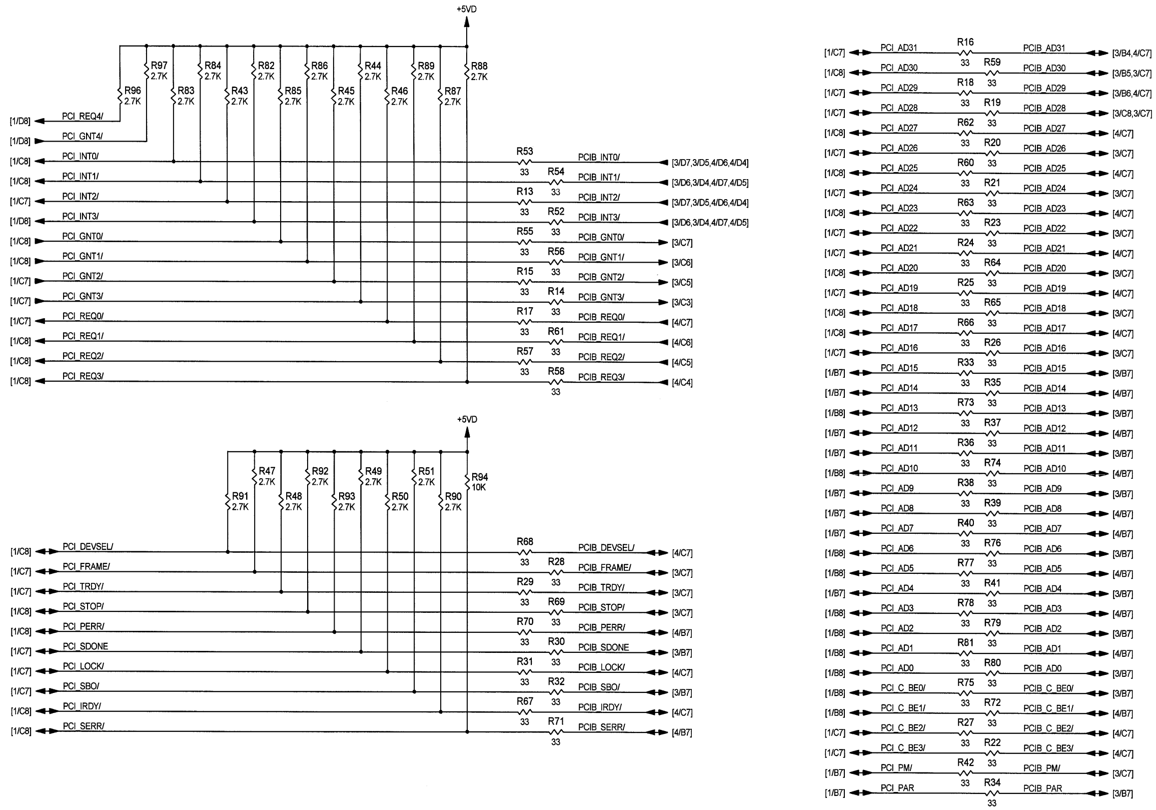
Drawings:

COMPONENT LAYOUT, PC BD, NLX BPL, 960L
COMPONENT LAYOUT, PC BD, I/O BPL, 960L
COMPONENT LAYOUT, PC BD, I/O CLK, 960L
COMPONENT LAYOUT, PC BD, AIN, 960L
COMPONENT LAYOUT, PC BD, AOUT, 960L
COMPONENT LAYOUT, PC BD, AES, 960L
COMPONENT LAYOUT, PC BD, RVB, 960L
COMPONENT LAYOUT, PC BD, MAIN, LARC2
080-13998 ASSY DWG,CHASSIS,960L
080-13999 ASSY DWG,SHIPMENT,960L
080-14403 ASSY DWG,PS CABLE HARNESS,960L
080-14231 ASSY DWG,MAIN HSG,LARC2
080-14232 ASSY DWG,DSPLY HSG,LARC2,SHARP
080-14233 ASSY DWG,JOYSTICK,LARC2
080-14234 ASSY DWG,MECH,MAIN BD,LARC2
080-14242 ASSY DWG,DSPLY HSG,LARC2,KYO
080-14243 ASSY DWG,SHIPMENT,LARC2

Your Notes:

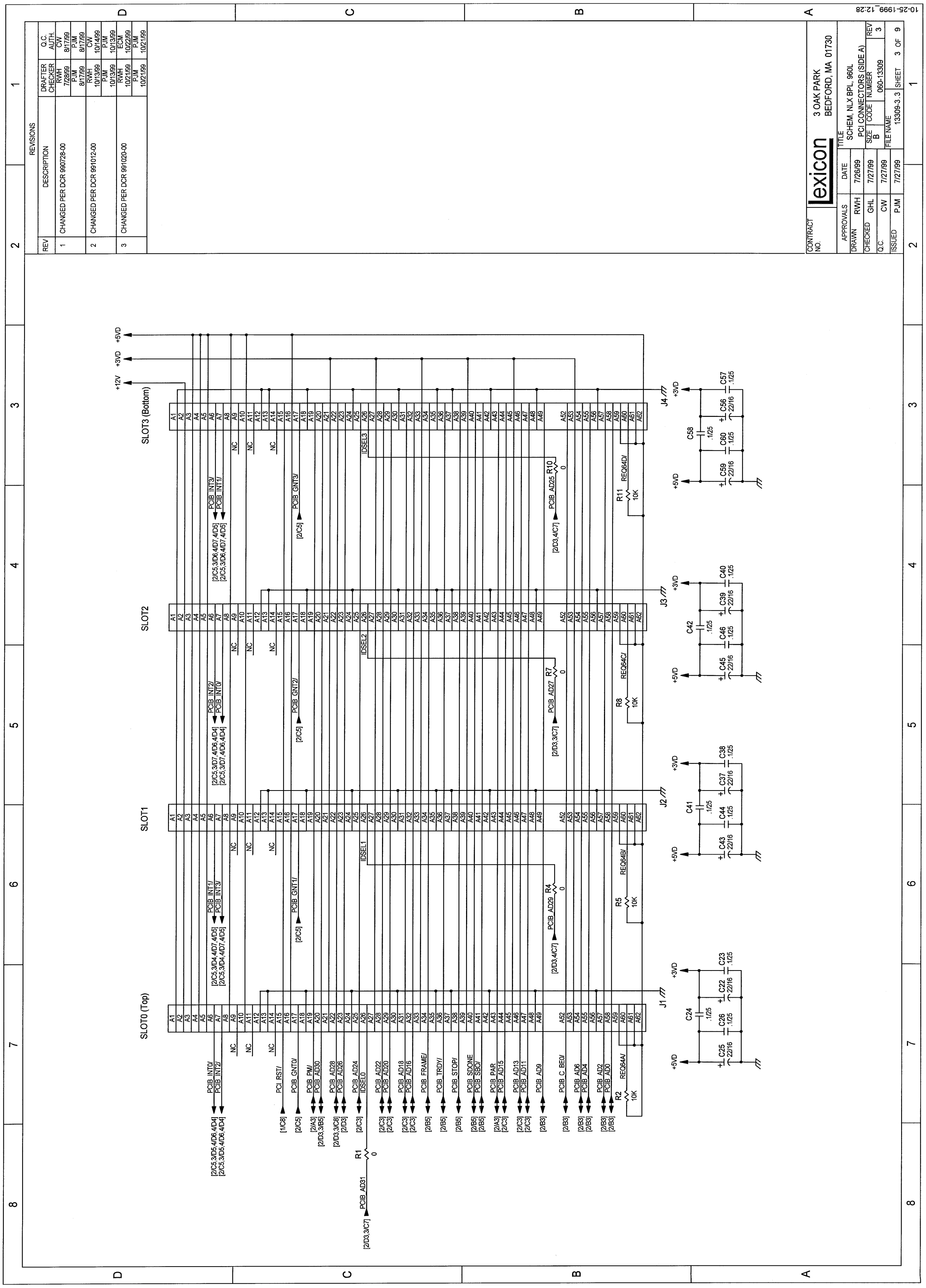

NLX CONNECTOR
J6
NOTES
1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]
6. COMPONENTS MARKED WITH * ARE NOT INSTALLED
7 LAST REFERENCE DESIGNATORS USED: C124, F1, FB6, J28, R164, U3
DOCUMENT CONTROL BLOCK #060-13309
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, NLX BPL 960L
NLX CONNECTOR
060-13309
13309-4.1
SHEET 1 OF 9

REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 990728-00	RWH 7/28/99 / PJM 8/17/99	CW 8/17/99 / PJM 8/17/99
2	CHANGED PER DCR 991012-00	RWH 10/13/99 / PJM 10/13/99	CW 10/14/99 / PJM 10/13/99
3	CHANGED PER DCR 991020-00	RWH 10/21/99 / PJM 10/21/99	ECM 10/22/99 / PJM 10/21/99

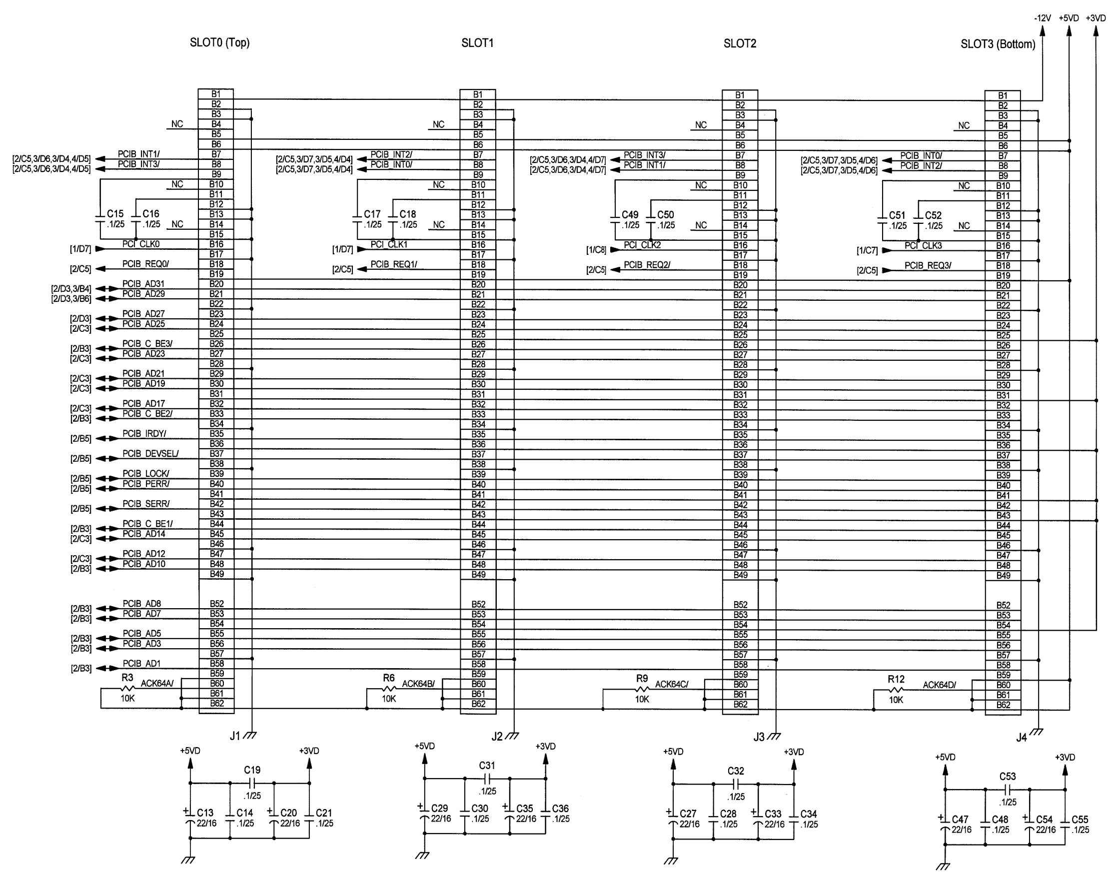


CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE SCHEM, NLX BPL, 960L PCI SERIES RESISTORS
DRAWN	RWH	7/26/99	
CHECKED	GHL	7/27/99	SIZE B / CODE / NUMBER 060-13309 / REV 3
Q.C.	CW	7/27/99	
ISSUED	PJM	7/27/99	FILE NAME 13309-3.2 / SHEET 2 OF 9

10-25-1999_11:39



SLOT0 (Top)
SLOT1
SLOT2
SLOT3 (Bottom)
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, NLX BPL, 960L
PCI CONNECTORS (SIDE A)
060-13309
13309-3.3



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 990728-00	RWH 7/28/99 PJM 8/17/99	CW 8/17/99 PJM 8/17/99
2	CHANGED PER DCR 991012-00	RWH 10/13/99 PJM 10/13/99	CW 10/14/99 PJM 10/13/99
3	CHANGED PER DCR 991020-00	RWH 10/21/99 PJM 10/21/99	ECM 10/22/99 PJM 10/21/99

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

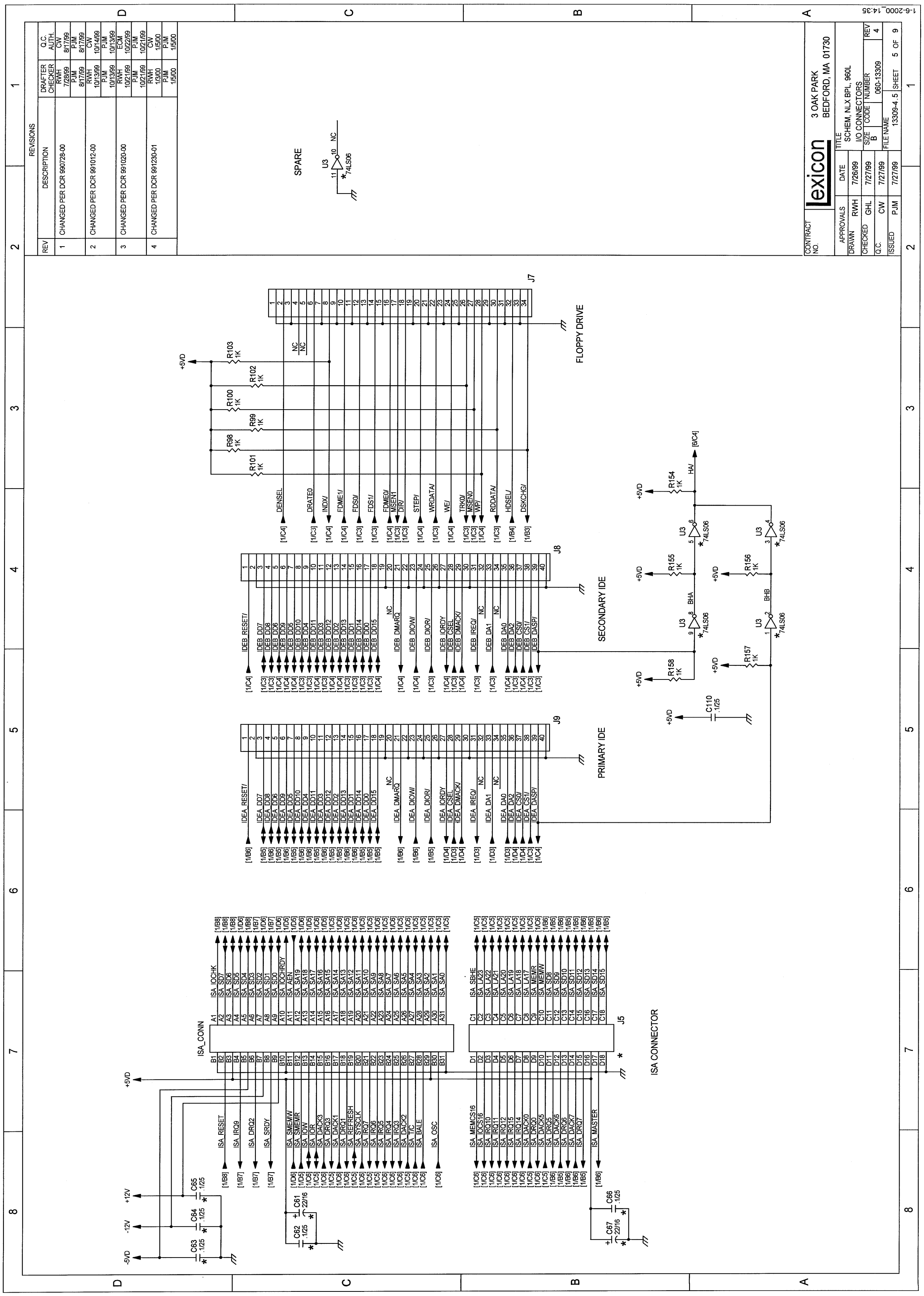
APPROVALS		DATE
DRAWN	RWH	7/26/99
CHECKED	GHL	7/27/99
Q.C.	CW	7/27/99
ISSUED	PJM	7/27/99

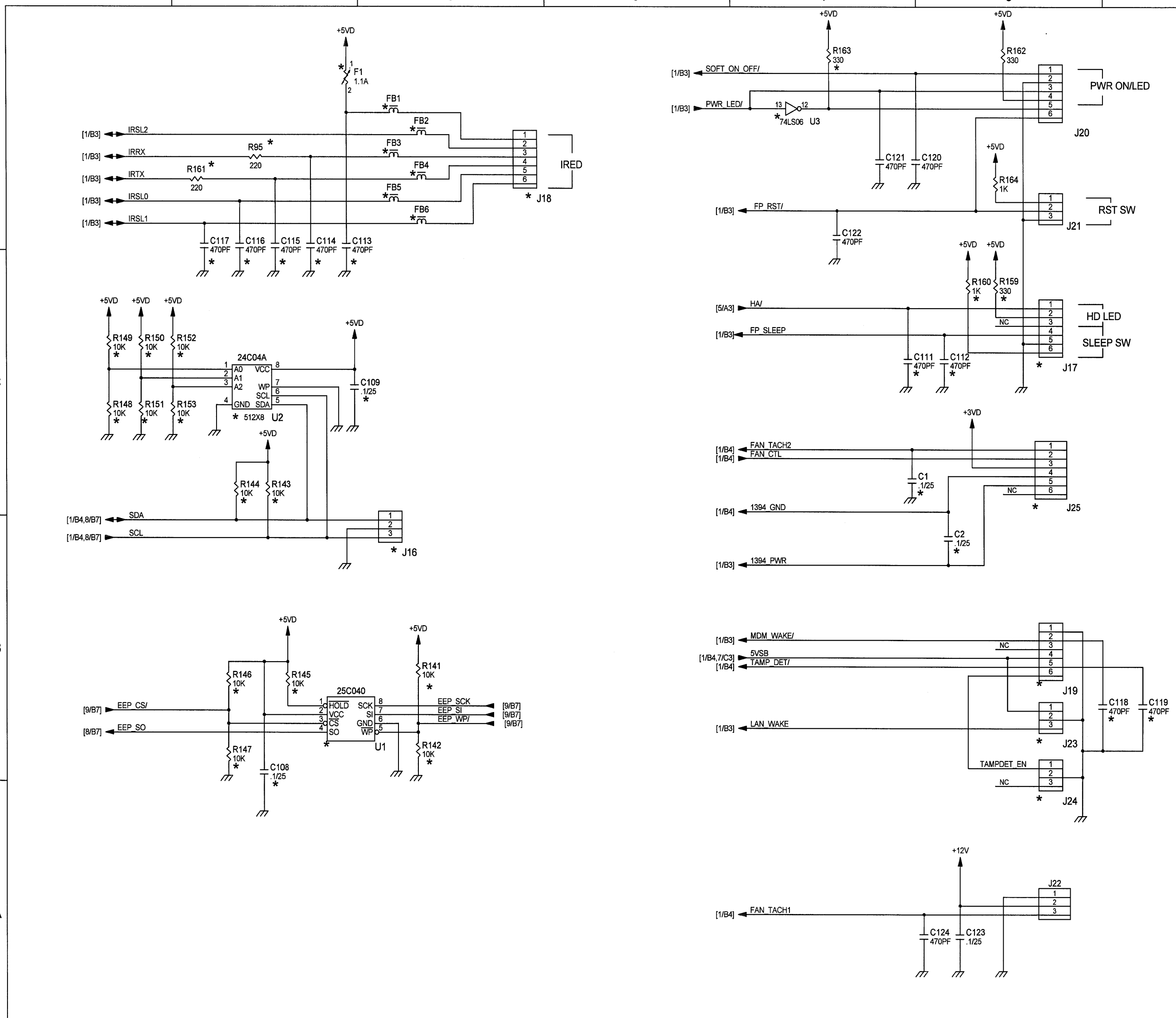
TITLE SCHEM, NLX BPL, 960L PCI CONNECTORS (SIDE B)

SIZE B CODE NUMBER 060-13309 REV 3

FILE NAME 13309-3.4 SHEET 4 OF 9

10-25-1999_12:29


SPARE
FLOPPY DRIVE
SECONDARY IDE
PRIMARY IDE
ISA CONNECTOR
3 OAK PARK
BEDFORD, MA 01730
SCHEM, NLX BPL, 960L
I/O CONNECTORS
060-13309
SHEET 5 OF 9



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 990728-00	RWH 7/28/99 PJM 8/17/99	CW 8/17/99 PJM 8/17/99
2	CHANGED PER DCR 991012-00	RWH 10/13/99 PJM 10/13/99	CW 10/14/99 PJM 10/13/99
3	CHANGED PER DCR 991020-00	RWH 10/21/99 PJM 10/21/99	ECM 10/22/99 PJM 10/21/99
4	CHANGED PER DCR 991230-01	RWH 1/3/00 PJM 1/5/00	CW 1/5/00 PJM 1/5/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

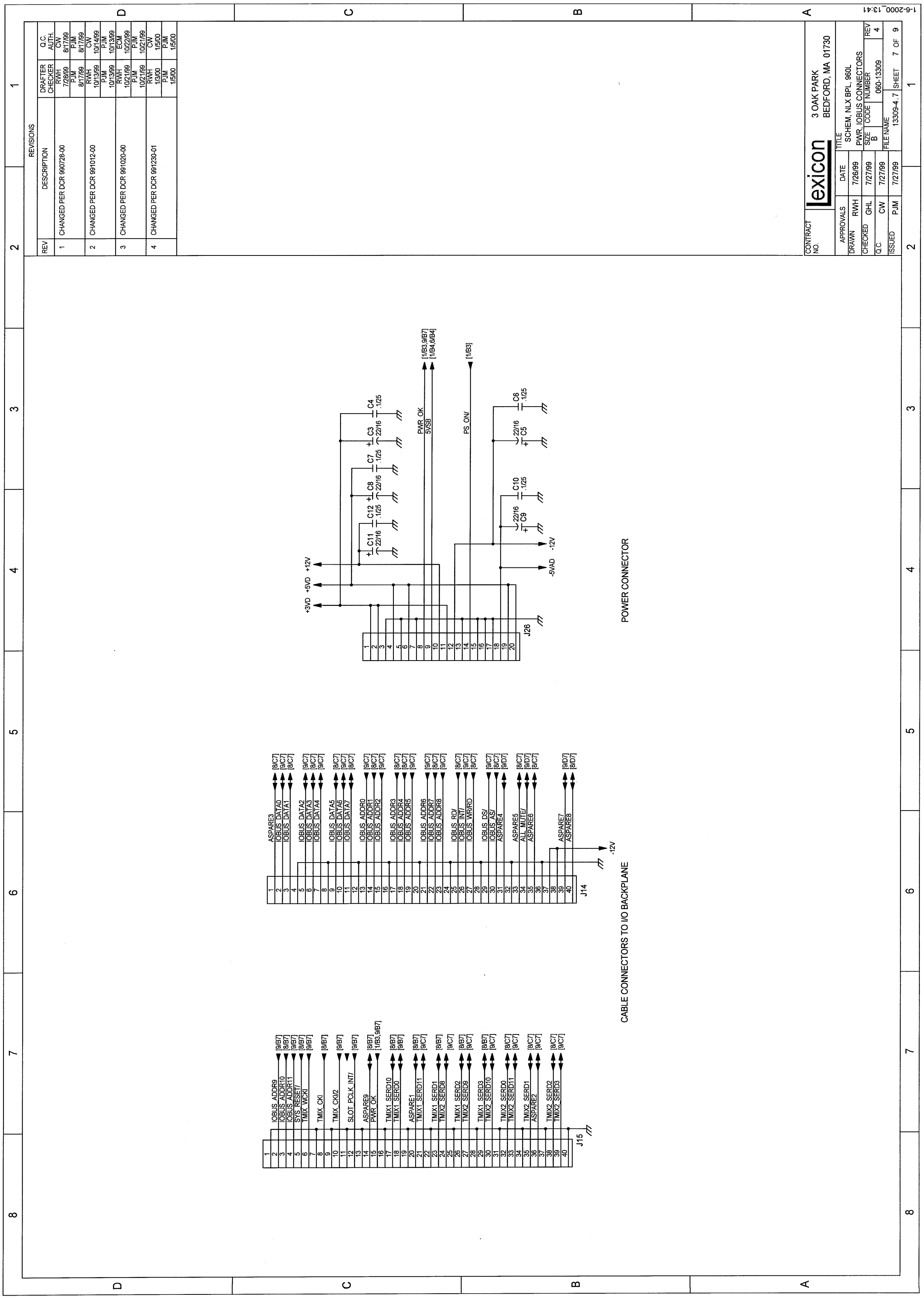
APPROVALS		DATE
DRAWN	RWH	7/26/99
CHECKED	GHL	7/27/99
Q.C.	CW	7/27/99
ISSUED	PJM	7/27/99

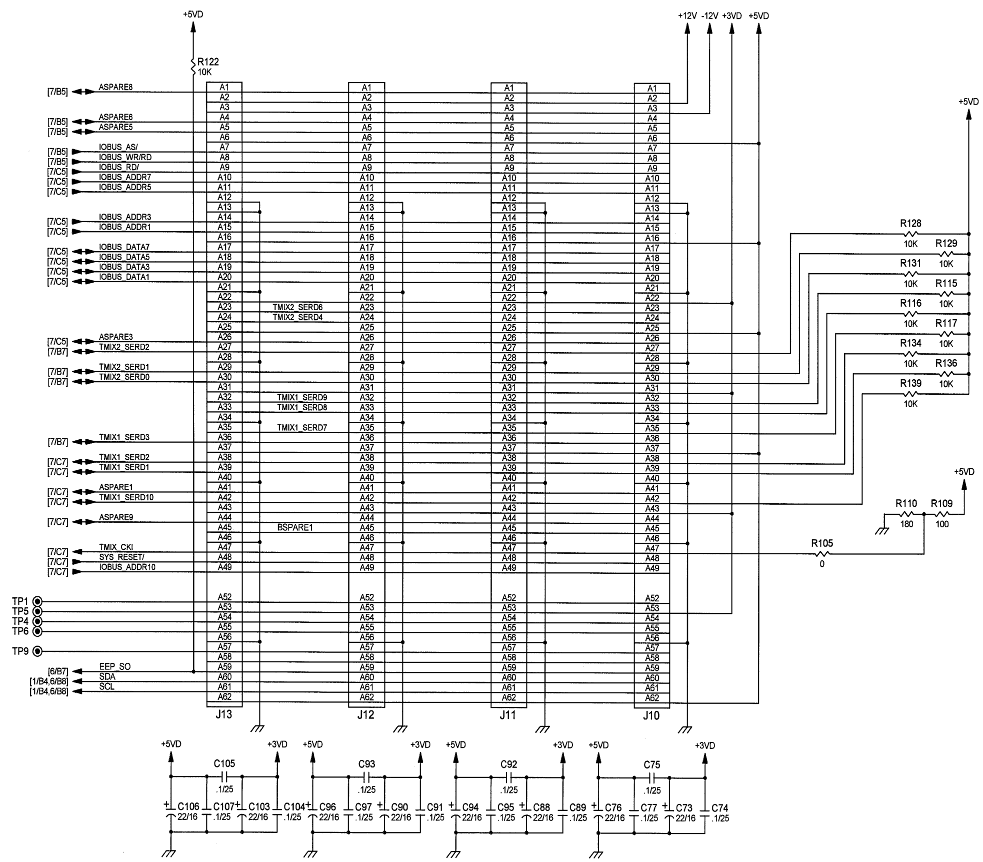
TITLE SCHEM, NLX BPL, 960L MISC CONNECTORS

SIZE B CODE NUMBER 060-13309 REV 4

FILE NAME 13309-4.6 SHEET 6 OF 9

1-6-2000_14:35


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 CHANGED PER DCR 990728-00 RWH 7/28/99 CW 8/17/99 PJM 8/17/99 PJM 8/17/99
2 CHANGED PER DCR 991012-00 RWH 10/13/99 CW 10/14/99 PJM 10/13/99 PJM 10/13/99
3 CHANGED PER DCR 991020-00 RWH 10/21/99 ECM 10/22/99 PJM 10/21/99 PJM 10/21/99
4 CHANGED PER DCR 991230-01 RWH 1/3/00 CW 1/5/00 PJM 1/5/00 PJM 1/5/00
POWER CONNECTOR
J26
+3VD +5VD +12V
-5VAD -12V
PWR_OK
5VSB
PS_ON/
CABLE CONNECTORS TO I/O BACKPLANE
J14
J15
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS DATE
DRAWN RWH 7/26/99
CHECKED GHL 7/27/99
Q.C. CW 7/27/99
ISSUED PJM 7/27/99
TITLE
SCHEM, NLX BPL, 960L
PWR, IOBUS CONNECTORS
SIZE B
CODE
NUMBER 060-13309
REV 4
FILE NAME 13309-4.7
SHEET 7 OF 9
1-6-2000_13:41



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 990728-00	RWH 7/28/99 PJM 8/17/99	CW 8/17/99 PJM 8/17/99
2	CHANGED PER DCR 991012-00	RWH 10/13/99 PJM 10/13/99	CW 10/14/99 PJM 10/13/99
3	CHANGED PER DCR 991020-00	RWH 10/21/99 PJM 10/21/99	ECM 10/22/99 PJM 10/21/99
4	CHANGED PER DCR 991230-01	RWH 1/3/00 PJM 1/5/00	CW 1/5/00 PJM 1/5/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

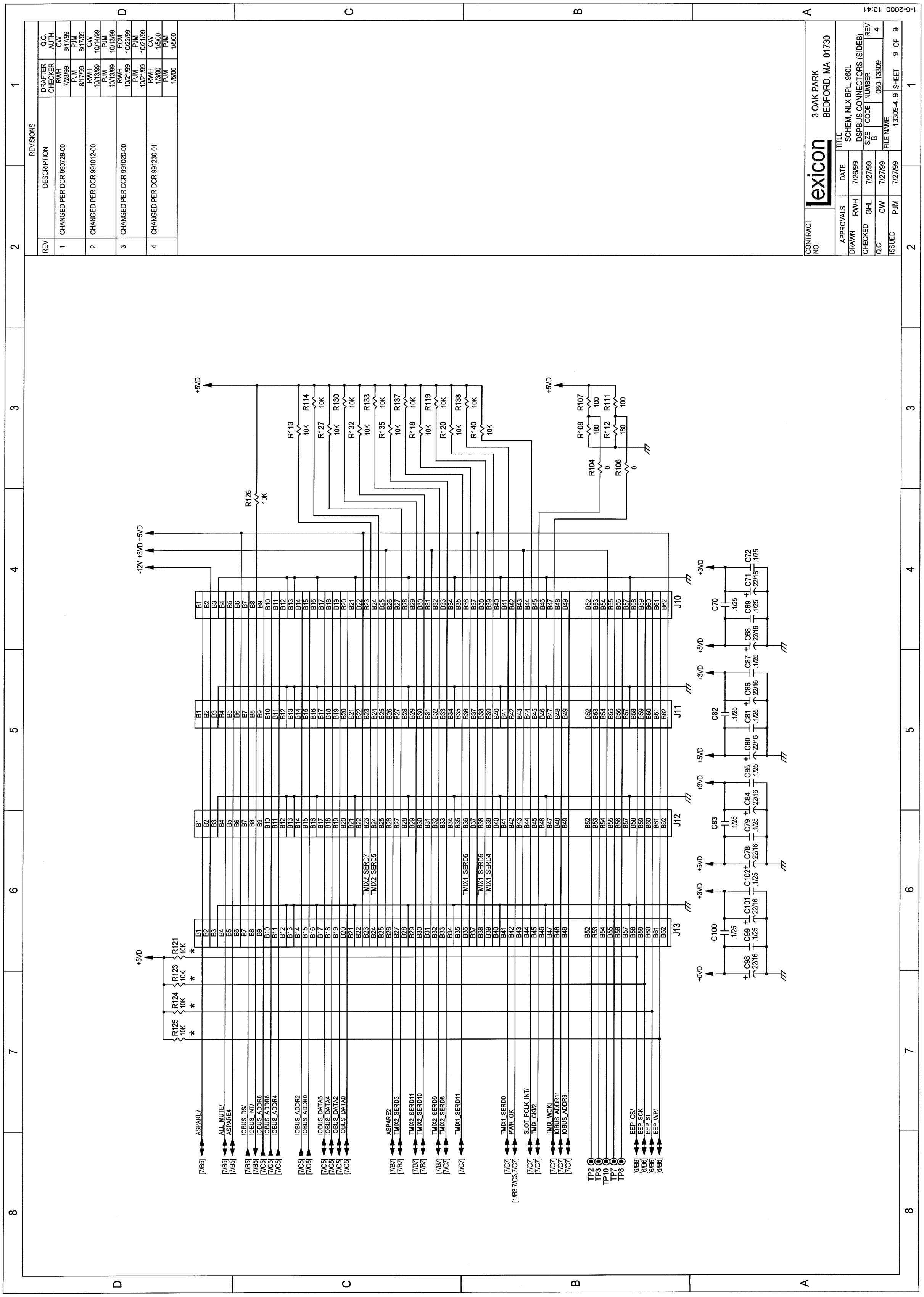
APPROVALS		DATE
DRAWN	RWH	7/26/99
CHECKED	GHL	7/27/99
Q.C.	CW	7/27/99
ISSUED	PJM	7/27/99

TITLE SCHEM, NLX BPL, 960L DSPBUS CONNECTORS (SIDE A)

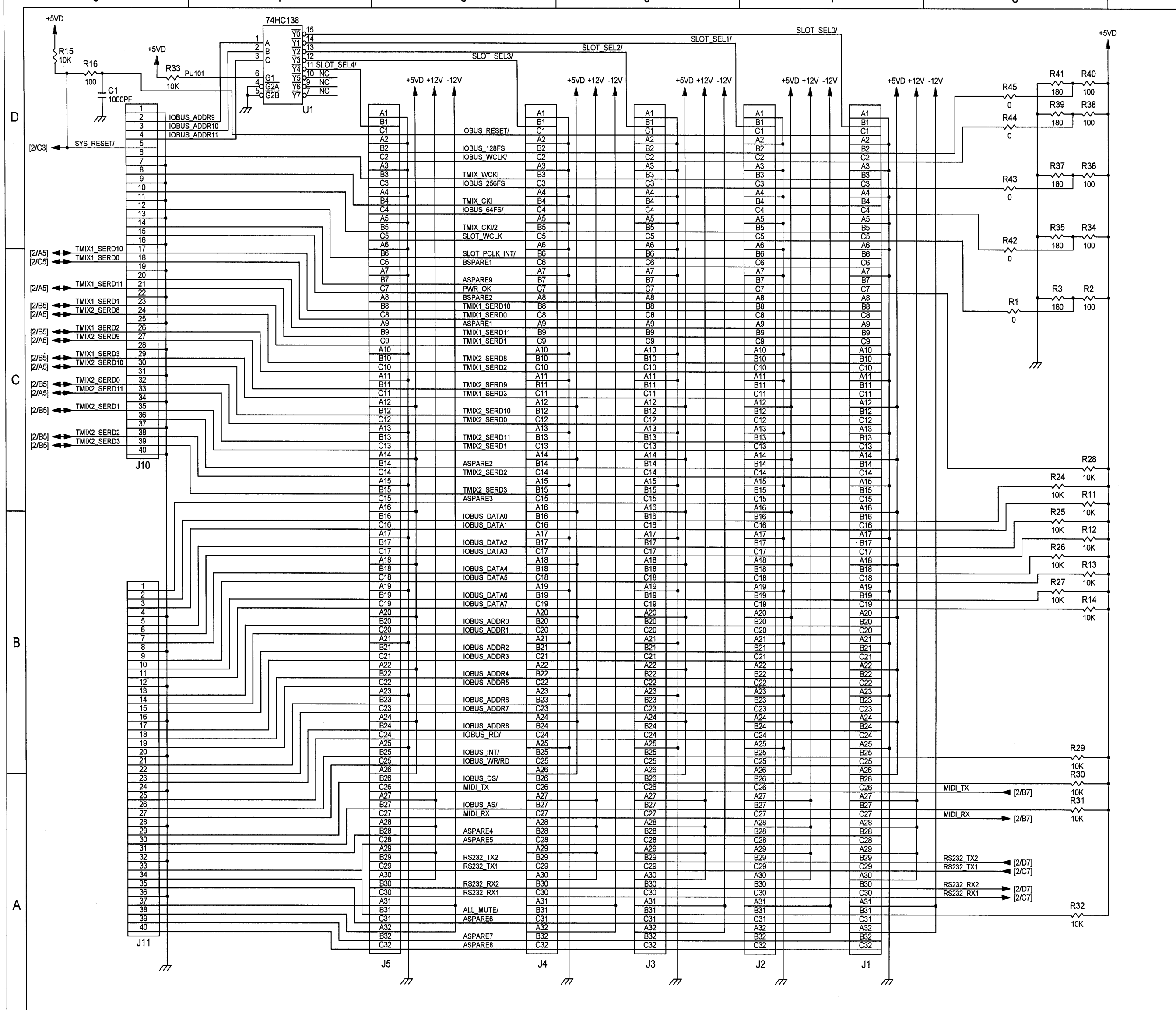
SIZE B | CODE | NUMBER 060-13309 | REV 4

FILE NAME 13309-4.8 | SHEET 8 OF 9

1-6-2000_13:41



REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 CHANGED PER DCR 990728-00
2 CHANGED PER DCR 991012-00
3 CHANGED PER DCR 991020-00
4 CHANGED PER DCR 991230-01
lexicon
3 OAK PARK
BEDFORD, MA 01730
TITLE
SCHEM, NLX BPL, 960L
DSPBUS CONNECTORS (SIDEB)
SIZE B
NUMBER 060-13309
REV 4
FILE NAME 13309-4.9
SHEET 9 OF 9
APPROVALS
DRAWN RWH 7/26/99
CHECKED GHL 7/27/99
Q.C. CW 7/27/99
ISSUED PJM 7/27/99
J10
J11
J12
J13
1-6-2000_13:41



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 990728-01	RWH 7/28/99 PJM 8/17/99	CW 8/17/99 PJM 8/17/99
2	CHANGED PER DCR 991012-01	RWH 10/13/99 PJM 10/14/99	CW 10/14/99 PJM 10/14/99
3	CHANGED PER DCR 000103-00	RWH 1/3/00 PJM 1/4/00	CW 1/4/00 PJM 1/4/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND — ANALOG GROUND — CHASSIS GROUND — POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C23, J11, R45, U1

DOCUMENT CONTROL BLOCK: #060-13319

SHEET NUMBER	REVISION NUMBER
1 OF 2	3
2 OF 2	3

CONTRACT NO.

lexicon — 3 OAK PARK, BEDFORD, MA 01730

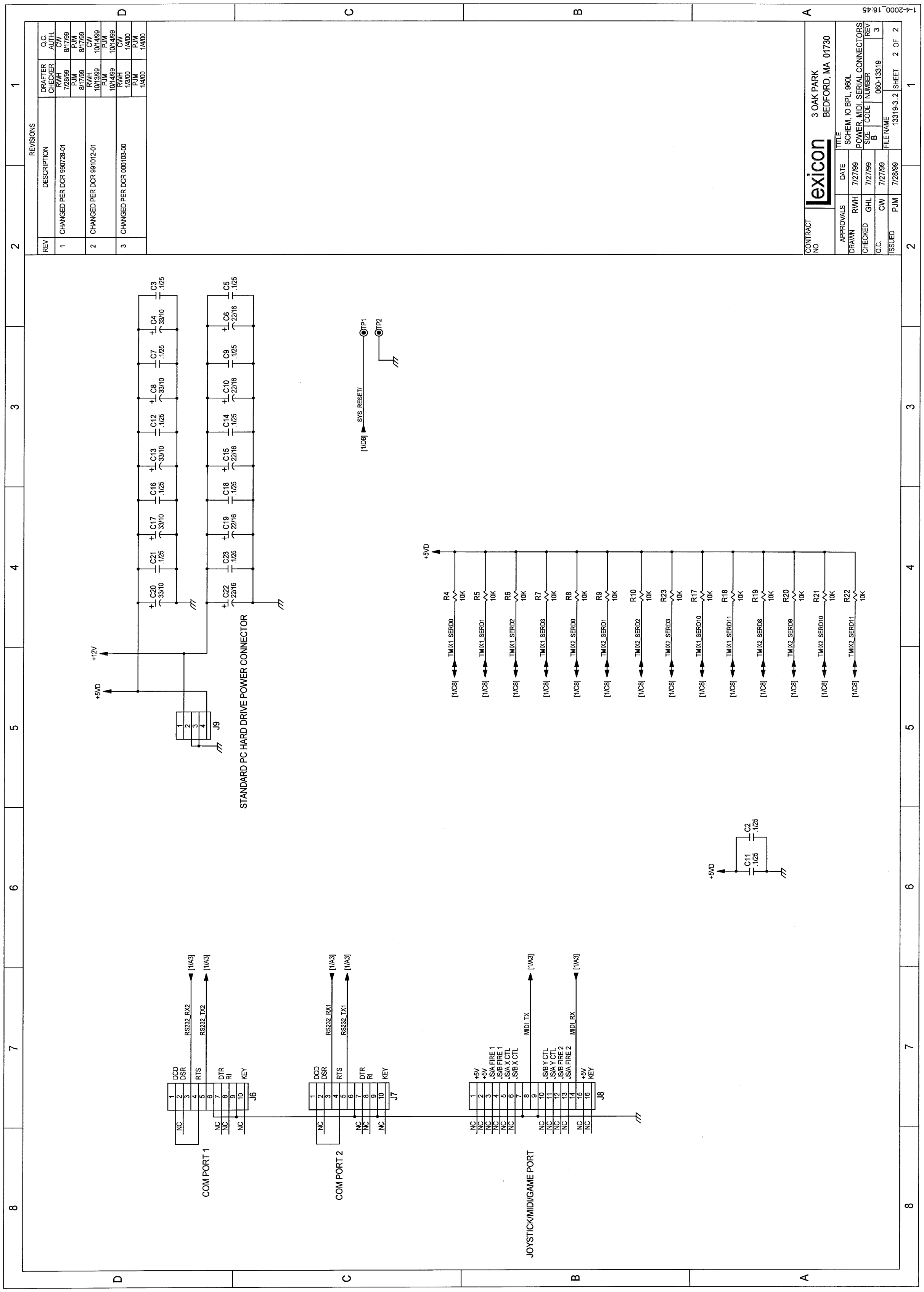
APPROVALS		DATE
DRAWN	RWH	7/27/99
CHECKED	GHL	7/27/99
Q.C.	CW	7/27/99
ISSUED	PJM	7/28/99

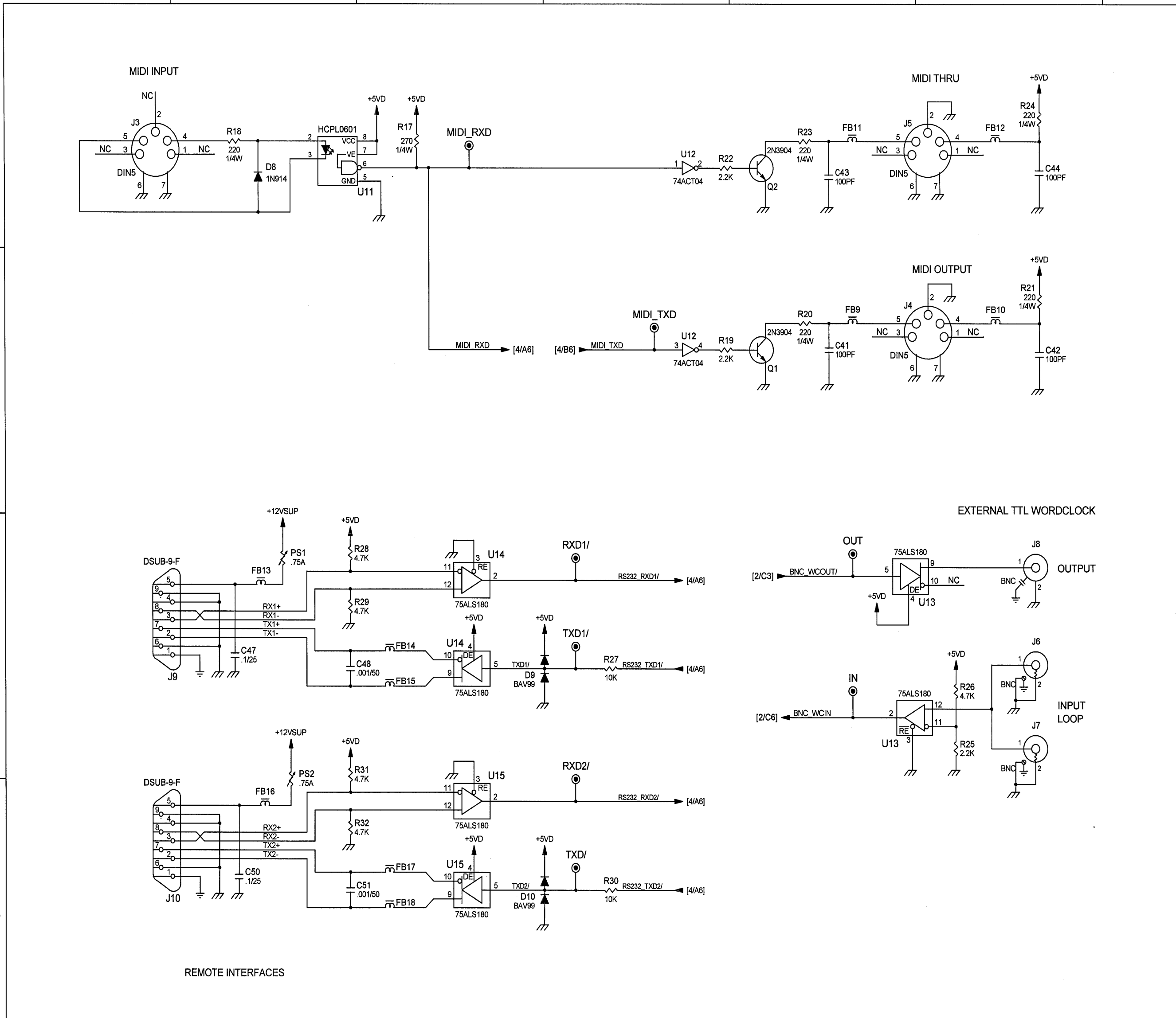
TITLE: SCHEM, IO BPL, 960L — I/O SLOT CONNECTORS

SIZE: B — CODE — NUMBER: 060-13319 — REV: 3

FILE NAME: 13319-3.1 — SHEET 1 OF 2

1-4-2000_16:45


STANDARD PC HARD DRIVE POWER CONNECTOR
COM PORT 1
COM PORT 2
JOYSTICK/MIDI/GAME PORT
3 OAK PARK
BEDFORD, MA 01730
SCHEM, IO BPL, 960L
POWER, MIDI, SERIAL CONNECTORS
060-13319
13319-3.2
SHEET 2 OF 2



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991105-00	RWH 11/11/99	CW 11/17/99
		ECM 11/17/99	PJM 11/18/99

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 LAST REFERENCE DESIGNATORS USED: C51, D10, FB18, FC1, J10, L1, PS2, Q2, R32, U15.

DOCUMENT CONTROL BLOCK: #060-13329

SHEET NUMBER	REVISION NUMBER
1 OF 4	1
2 OF 4	1
3 OF 4	1
4 OF 4	1

CONTRACT NO.

lexicon

3 OAK PARK
BEDFORD, MA 01730

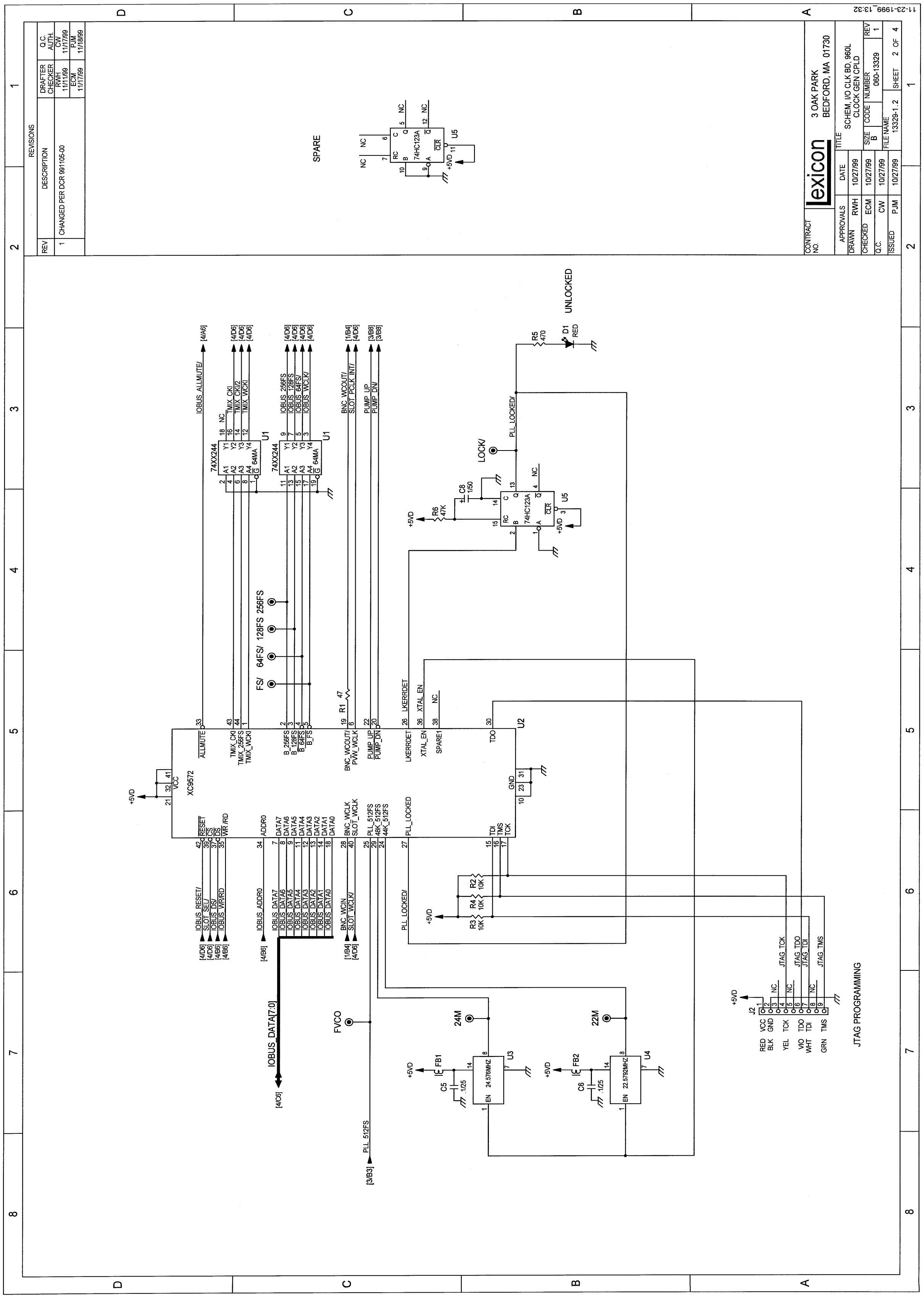
APPROVALS		DATE
DRAWN	RWH	10/27/99
CHECKED	ECM	10/27/99
Q.C.	CW	10/27/99
ISSUED	PJM	10/27/99

TITLE: SCHEM, I/O CLK BD, 960L I/O

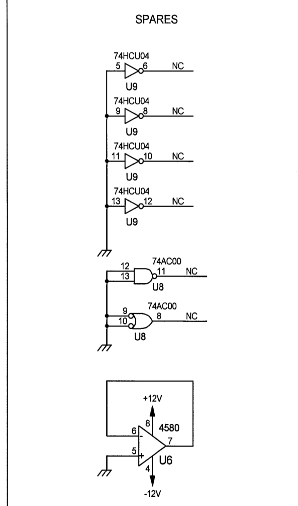
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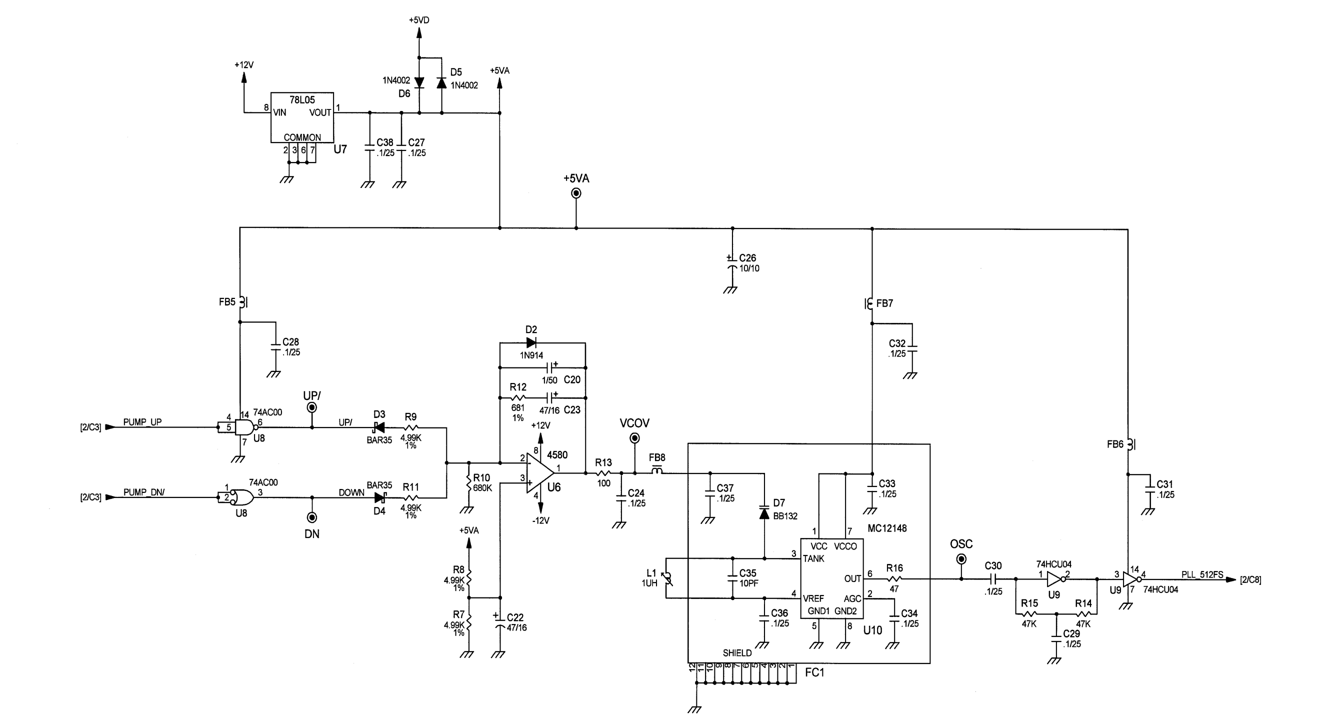
FILE NAME: 13329-1.1 | SHEET 1 OF 4

11-23-1999_13:55


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, I/O CLK BD, 960L
CLOCK GEN CPLD
060-13329
13329-1.2
SHEET 2 OF 4
11-23-1999_13:32
REVISIONS
CHANGED PER DCR 991105-00
XC9572
74XX244
74HC123A
SPARE
UNLOCKED
LOCK/
FVCO
24M
22M
IOBUS_DATA[7:0]
JTAG PROGRAMMING
FS/ 64FS/ 128FS 256FS

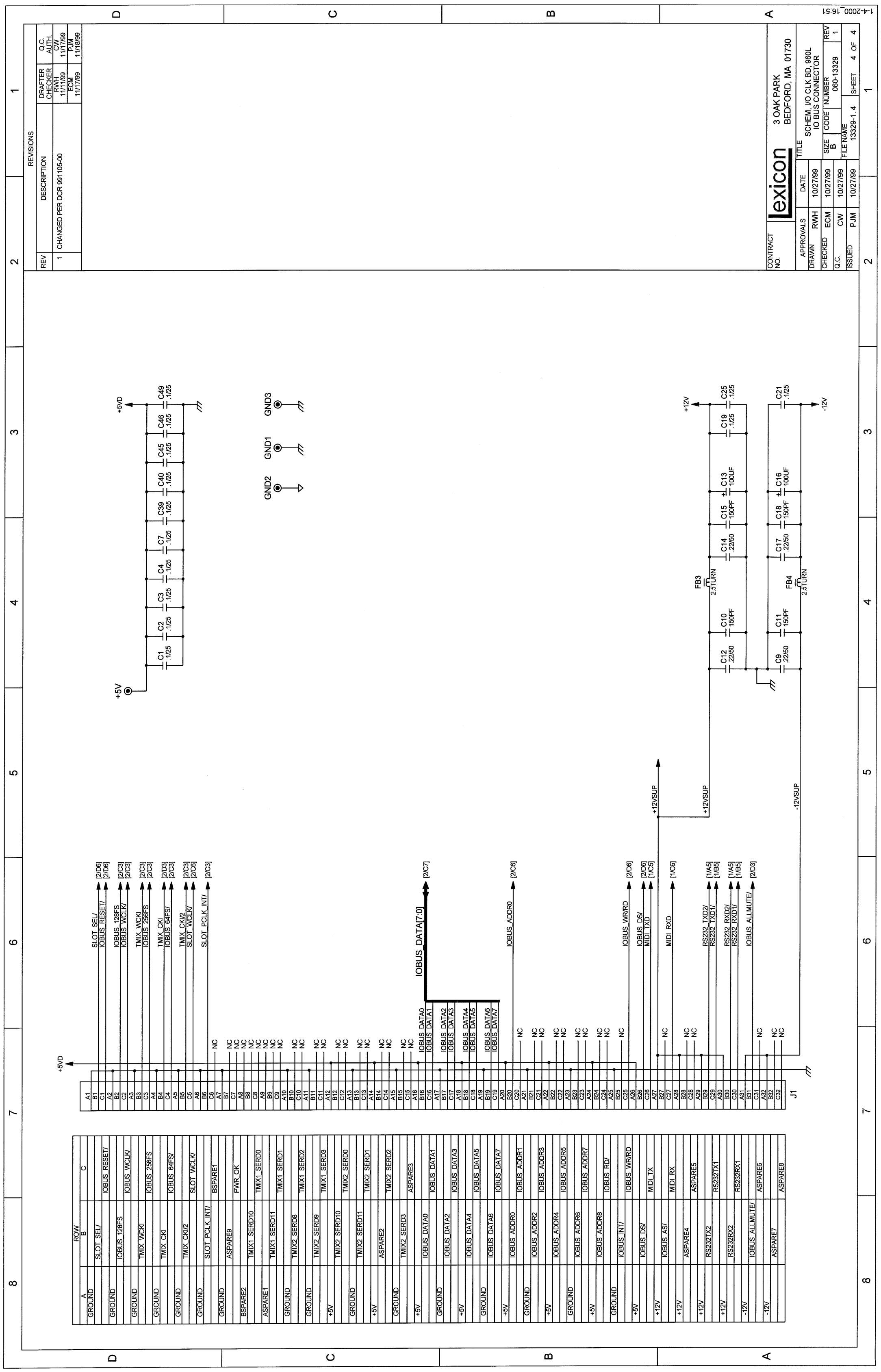
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991105-00	RWH 11/11/99 ECM 11/17/99	CW 11/17/99 PJM 11/18/99

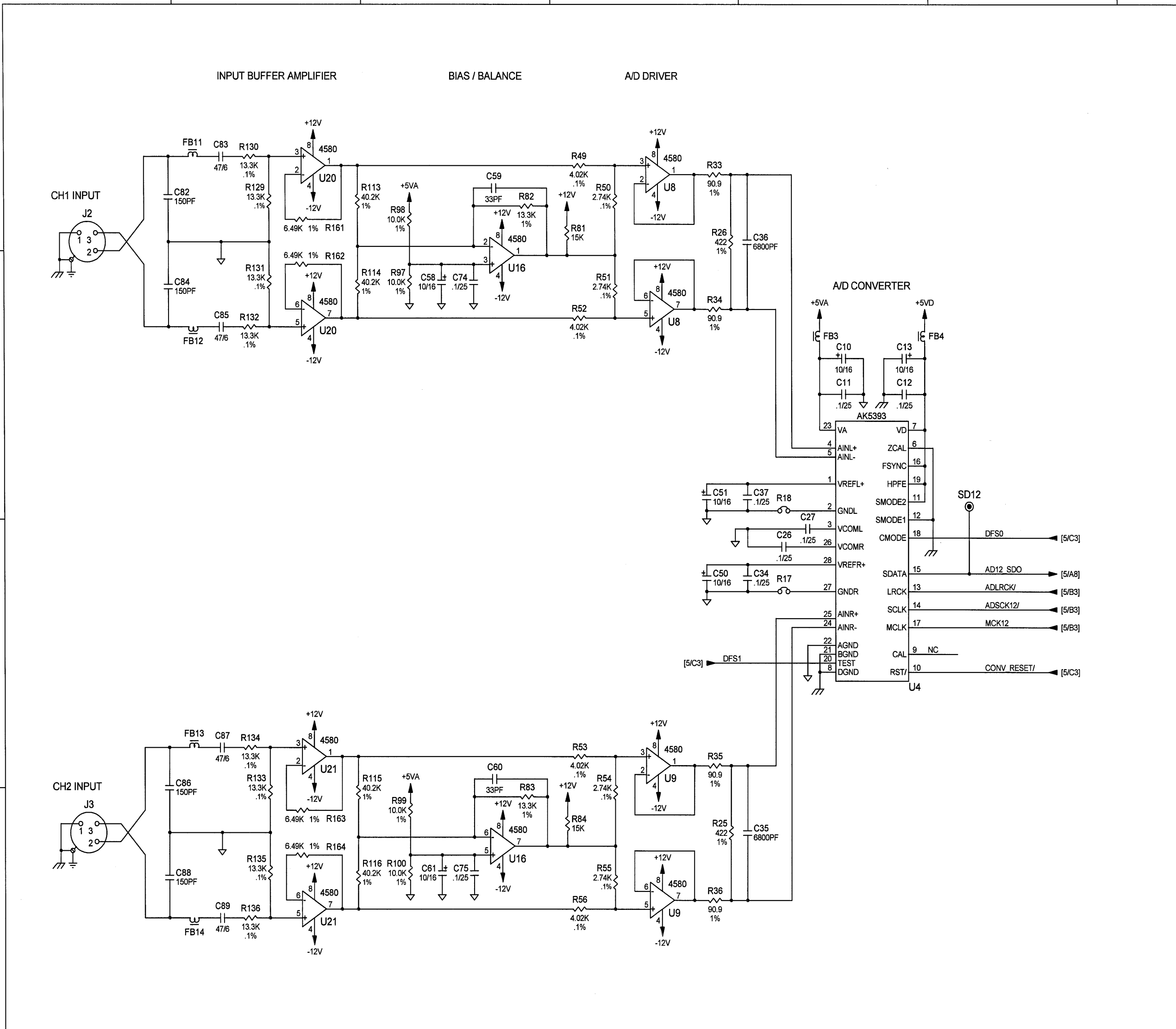




CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730			
APPROVALS		DATE	TITLE SCHEM, I/O CLK BD, 960L PLL		
DRAWN	RWH	10/27/99			
CHECKED	ECM	10/27/99	SIZE B	CODE	NUMBER 060-13329 REV 1
Q.C.	CW	10/27/99	FILE NAME 13329-1.3		SHEET 3 OF 4
ISSUED	PJM	10/27/99			

12-28-1999_16:01


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, I/O CLK BD, 960L
IO BUS CONNECTOR
060-13329
13329-1.4
REVISIONS
CHANGED PER DCR 991105-00



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991201-00	RWH 12/9/99 ECM 1/5/00	CW 1/5/00 PJM 1/5/00
2	CHANGED SHEET 7 PER ECO 000110-01	RWH 1/13/00 ECM 1/13/00	CW 1/14/00 PJM 1/14/00
3	ADDED R161-164; CHG SHEETS 2-4 PER ECO 000211-01	RWH 2/15/00 ECM 2/15/00	CW 2/15/00 PJM 2/15/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND; ANALOG GROUND; CHASSIS GROUND; POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 COMPONENTS MARKED WITH * ARE NOT INSTALLED

7 LAST REFERENCE DESIGNATORS USED: C113, D8, FB26, J9, R176, U27

DOCUMENT CONTROL BLOCK: #060-13339

SHEET NUMBER	REVISION NUMBER
1 OF 7	3
2 OF 7	2
3 OF 7	2
4 OF 7	2
5 OF 7	1
6 OF 7	1
7 OF 7	2

CONTRACT NO.

lexicon — 3 OAK PARK, BEDFORD, MA 01730

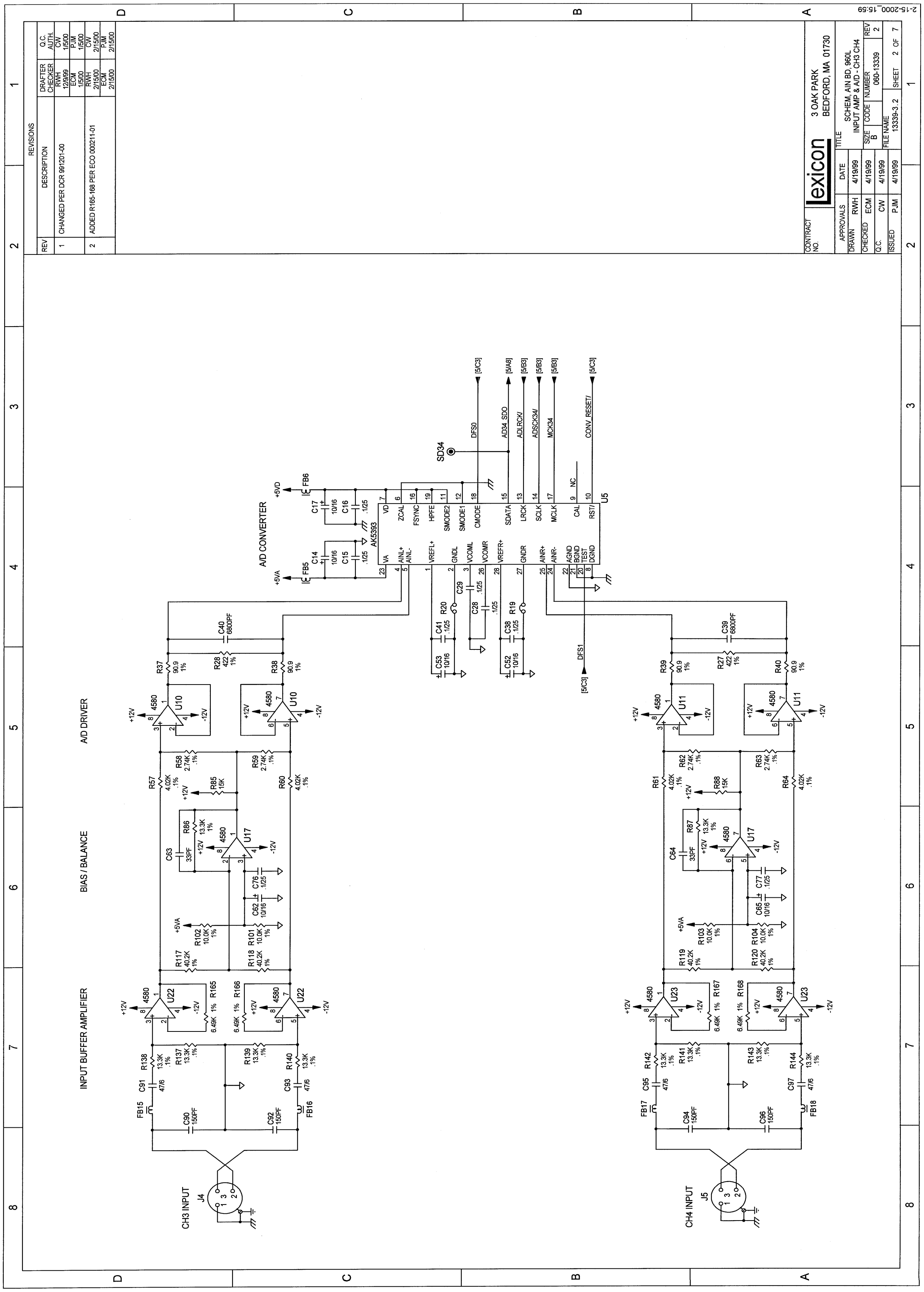
APPROVALS		DATE
DRAWN	RWH	4/19/99
CHECKED	ECM	4/19/99
Q.C.	CW	4/19/99
ISSUED	PJM	4/19/99

TITLE: SCHEM, AIN BD, 960L INPUT AMP & A/D - CH1 CH2

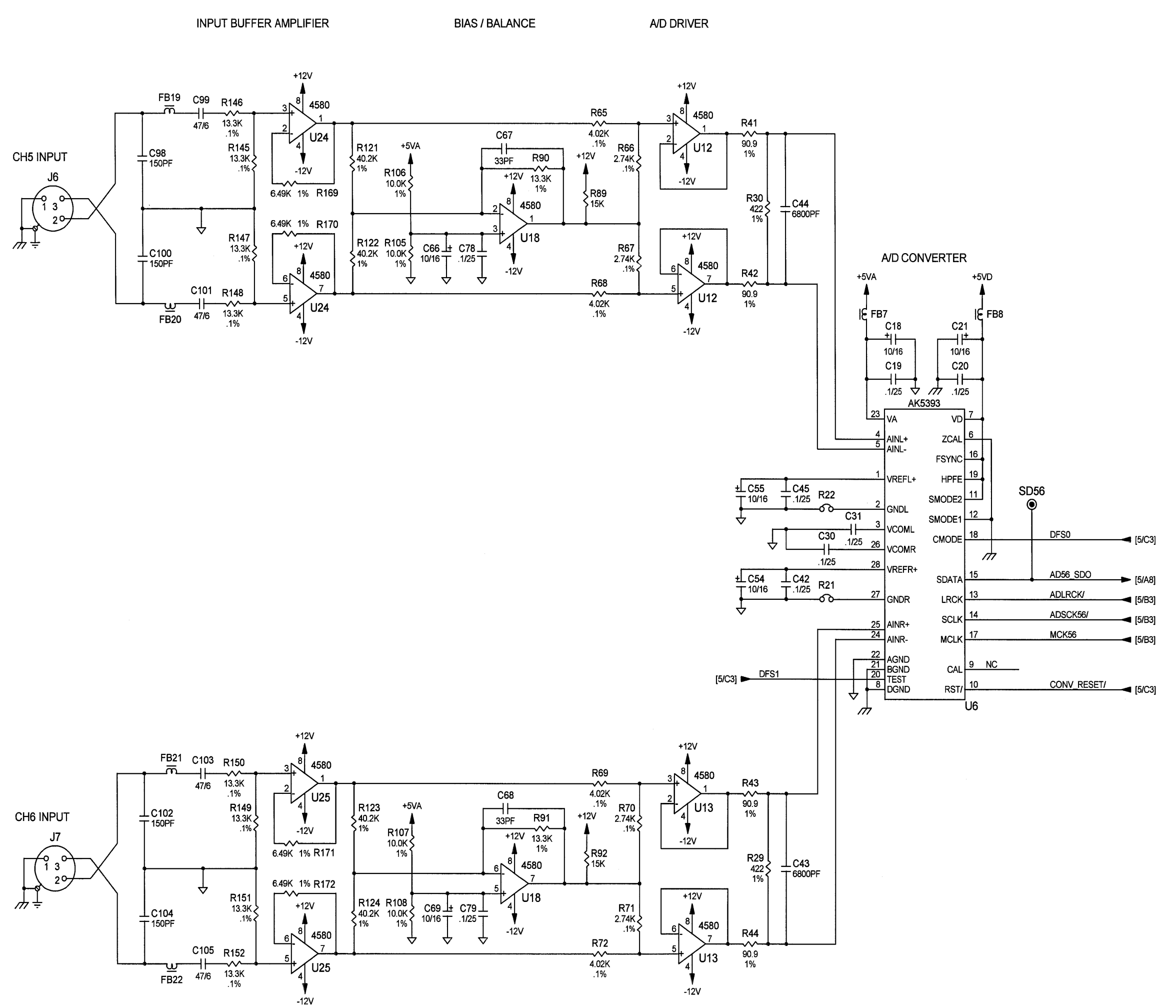
SIZE: B | CODE | NUMBER: 060-13339 | REV: 3

FILE NAME: 13339-3.1 | SHEET 1 OF 7

2-15-2000_15:58

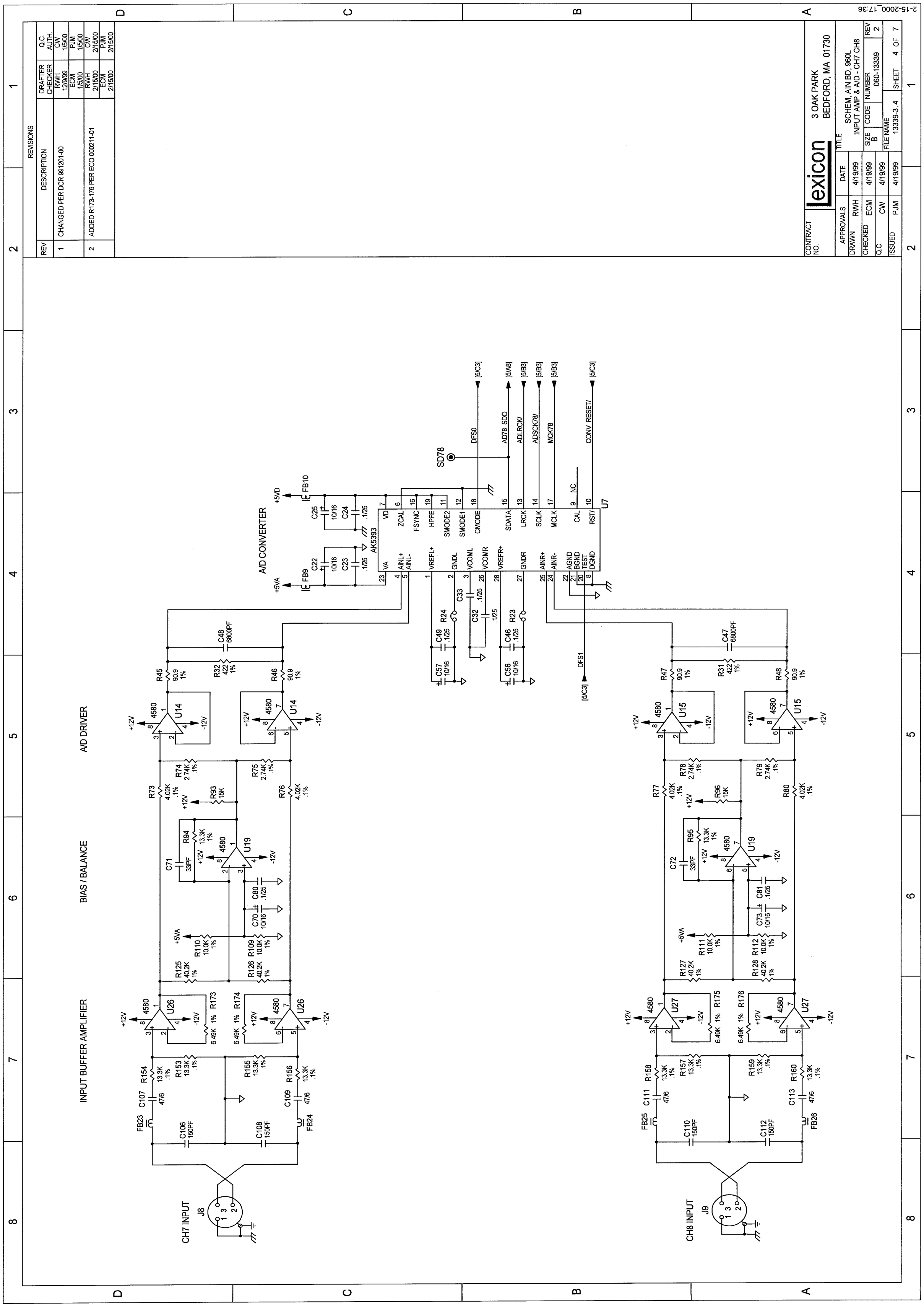

A/D CONVERTER
AK5393
A/D DRIVER
BIAS / BALANCE
INPUT BUFFER AMPLIFIER
CH3 INPUT
CH4 INPUT
REVISIONS
CHANGED PER DCR 991201-00
ADDED R165-168 PER ECO 000211-01
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AIN BD, 960L
INPUT AMP & A/D - CH3 CH4
060-13339
13339-3_2
SHEET 2 OF 7
2-15-2000 15:59

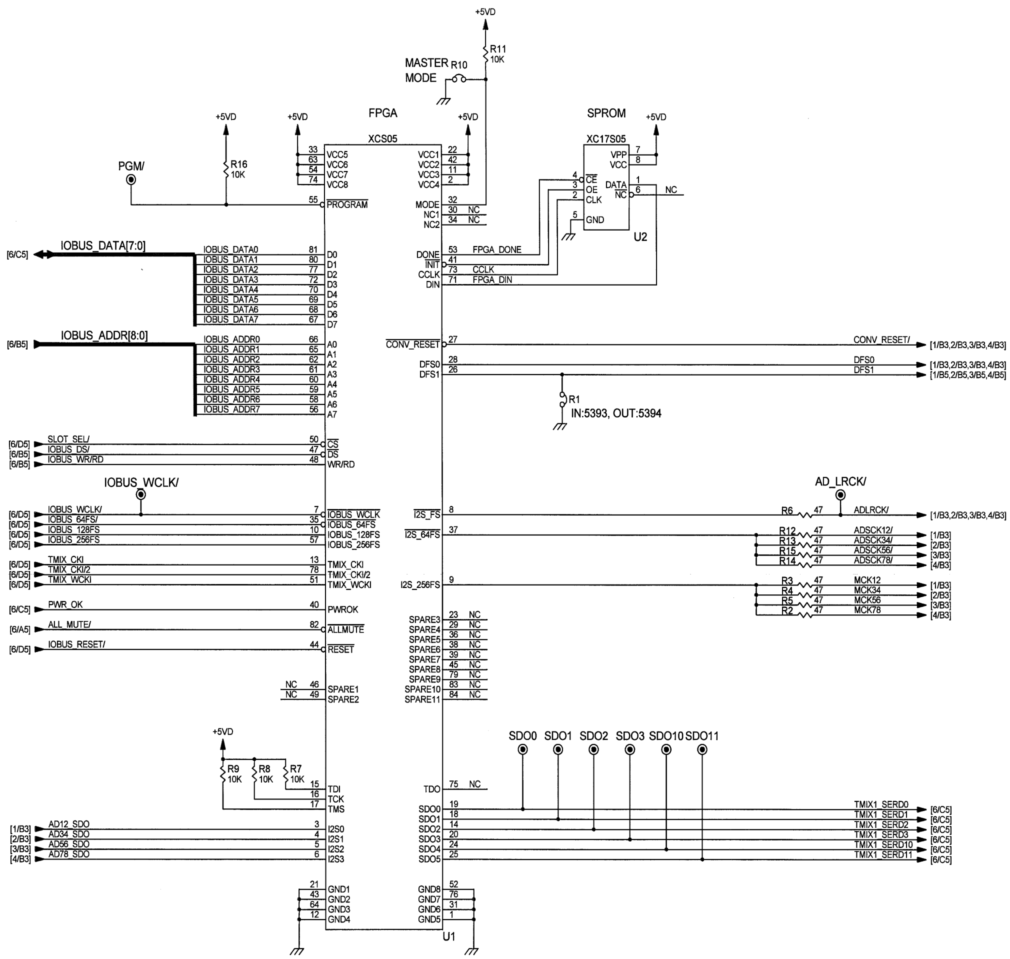
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH
1	CHANGED PER DCR 991201-00	RWH 12/9/99 ECM 1/5/00	CW 1/5/00 PJM 1/5/00
2	ADDED R169-172 PER ECO 000211-01	RWH 2/15/00 ECM 2/15/00	CW 2/15/00 PJM 2/15/00



CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS	DATE	TITLE SCHEM, AIN BD, 960L INPUT AMP & A/D - CH5 CH6	
DRAWN RWH	4/19/99		
CHECKED ECM	4/19/99	SIZE B / CODE / NUMBER 060-13339	REV 2
Q.C. CW	4/19/99	FILE NAME 13339-3.3	SHEET 3 OF 7
ISSUED PJM	4/19/99		

2-15-2000_15:59


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1 CHANGED PER DCR 991201-00
2 ADDED R173-176 PER ECO 000211-01
INPUT BUFFER AMPLIFIER
BIAS / BALANCE
A/D DRIVER
A/D CONVERTER
AK5393
CH7 INPUT
J8
CH8 INPUT
J9
SD78
DFS0
AD78_SDO
ADLRCK/
ADSCK78/
MCK78
CONV_RESET/
DFS1
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AIN BD, 960L
INPUT AMP & A/D - CH7 CH8
060-13339
13339-3_4
SHEET 4 OF 7
2-15-2000_17:36



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH
1	CHANGED PER DCR 991201-00	RWH 12/9/99 ECM 1/5/00	CW 1/5/00 PJM 1/5/00

CONTRACT NO.

lexicon — 3 OAK PARK, BEDFORD, MA 01730

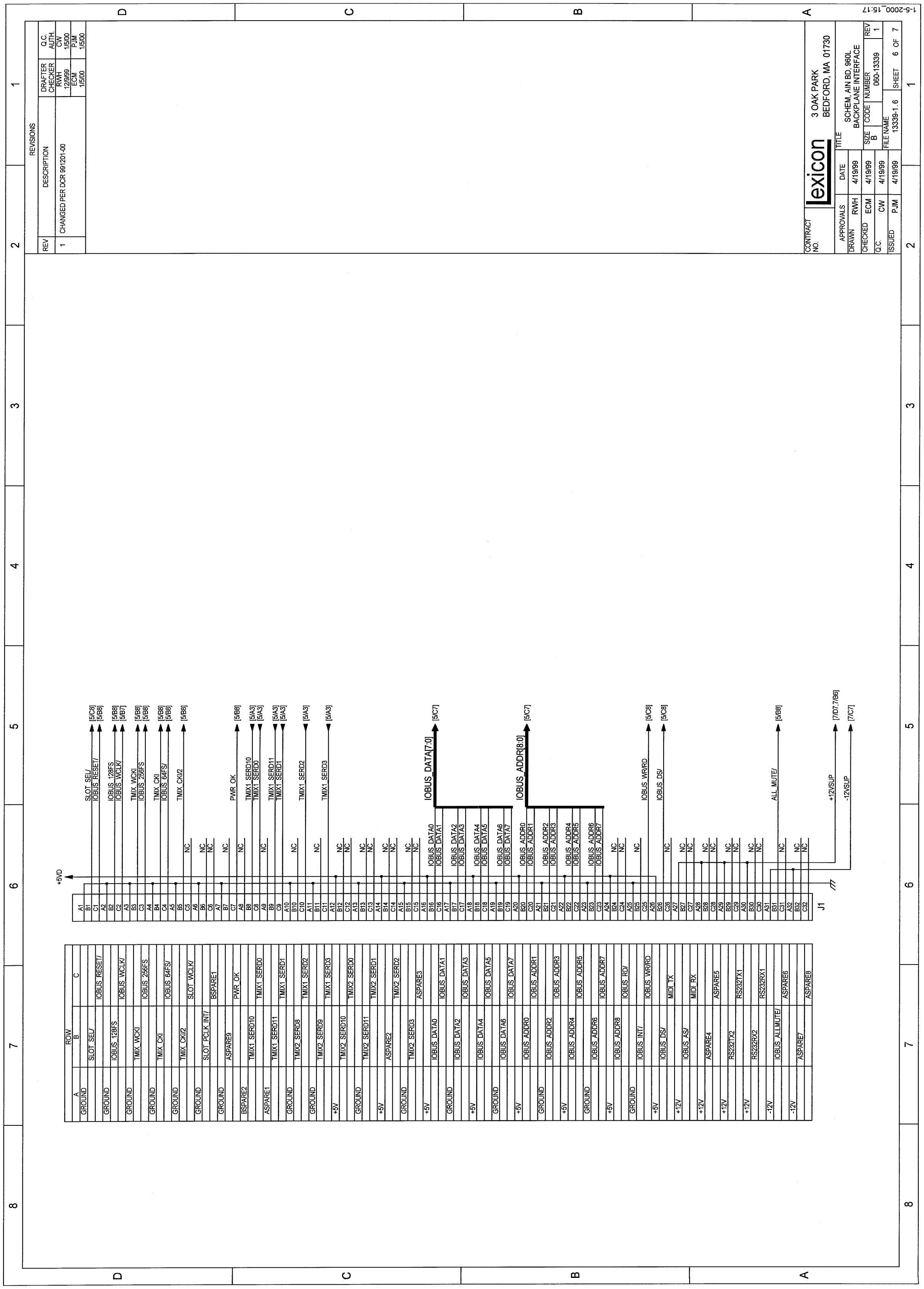
APPROVALS		DATE
DRAWN	RWH	4/19/99
CHECKED	ECM	4/19/99
Q.C.	CW	4/19/99
ISSUED	PJM	4/19/99

TITLE: SCHEM, AIN BD, 960L FPGA

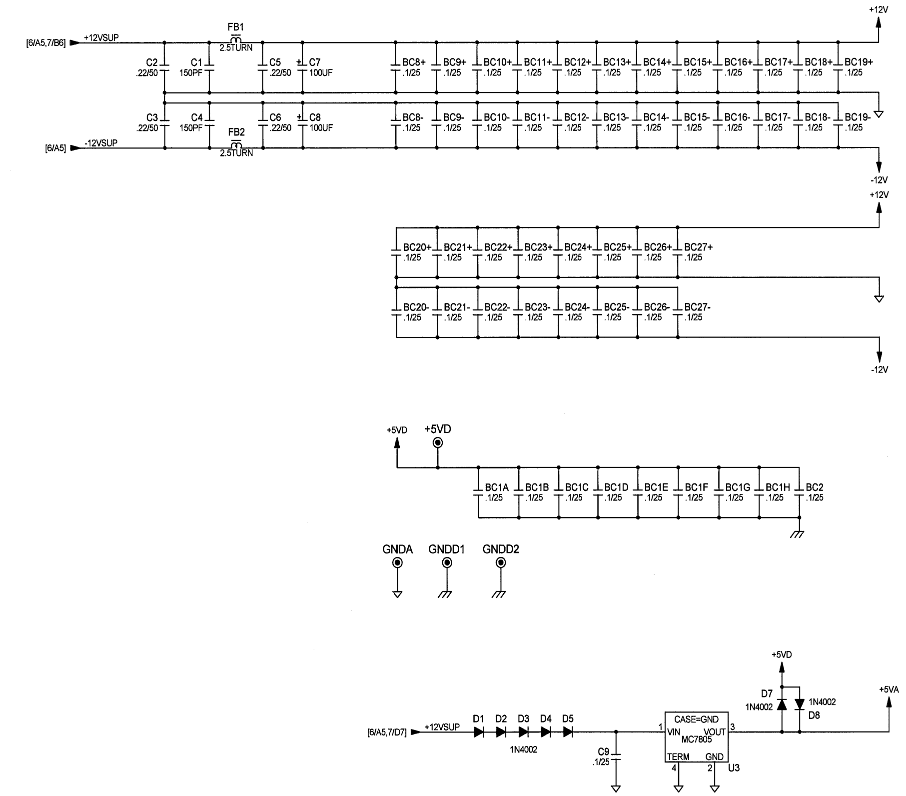
SIZE: B | CODE | NUMBER: 060-13339 | REV: 1

FILE NAME: 13339-1.5 | SHEET 5 OF 7

1-6-2000_13:37



3 OAK PARK
BEDFORD, MA 01730
SCHEM, AIN BD, 960L
BACKPLANE INTERFACE
060-13339
13339-1.6
SHEET 6 OF 7
CHANGED PER DCR 991201-00
J1
IOBUS_DATA[7:0]
IOBUS_ADDR[8:0]



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991201-00	RWH 12/9/99 ECM 1/5/00	CW 1/5/00 PJM 1/5/00
2	REMOVED D6 PER ECO 000110-01	RWH 1/13/00 ECM 1/13/00	CW 1/14/00 PJM 1/14/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

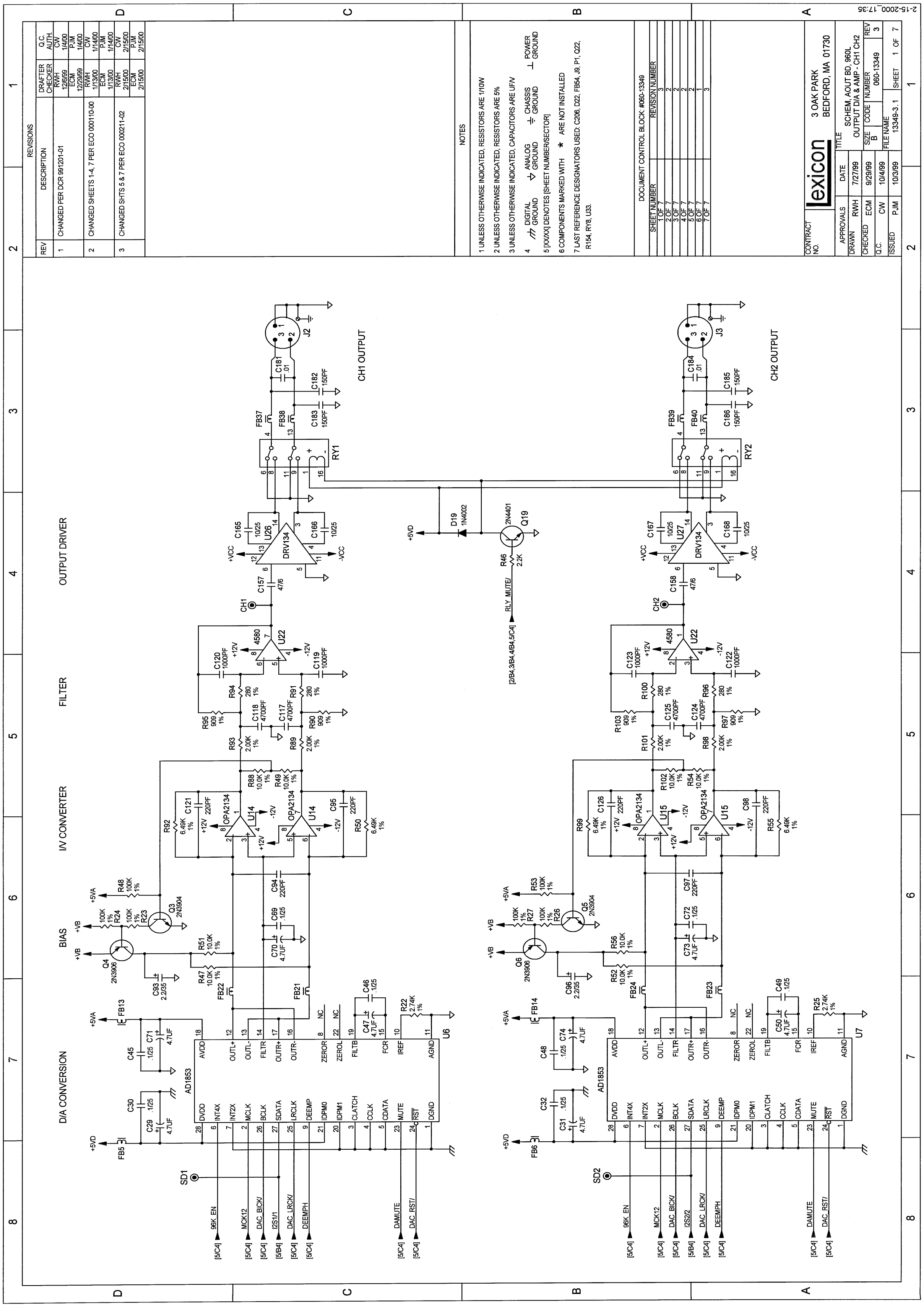
APPROVALS		DATE
DRAWN	RWH	4/19/99
CHECKED	ECM	4/19/99
Q.C.	CW	4/19/99
ISSUED	PJM	4/19/99

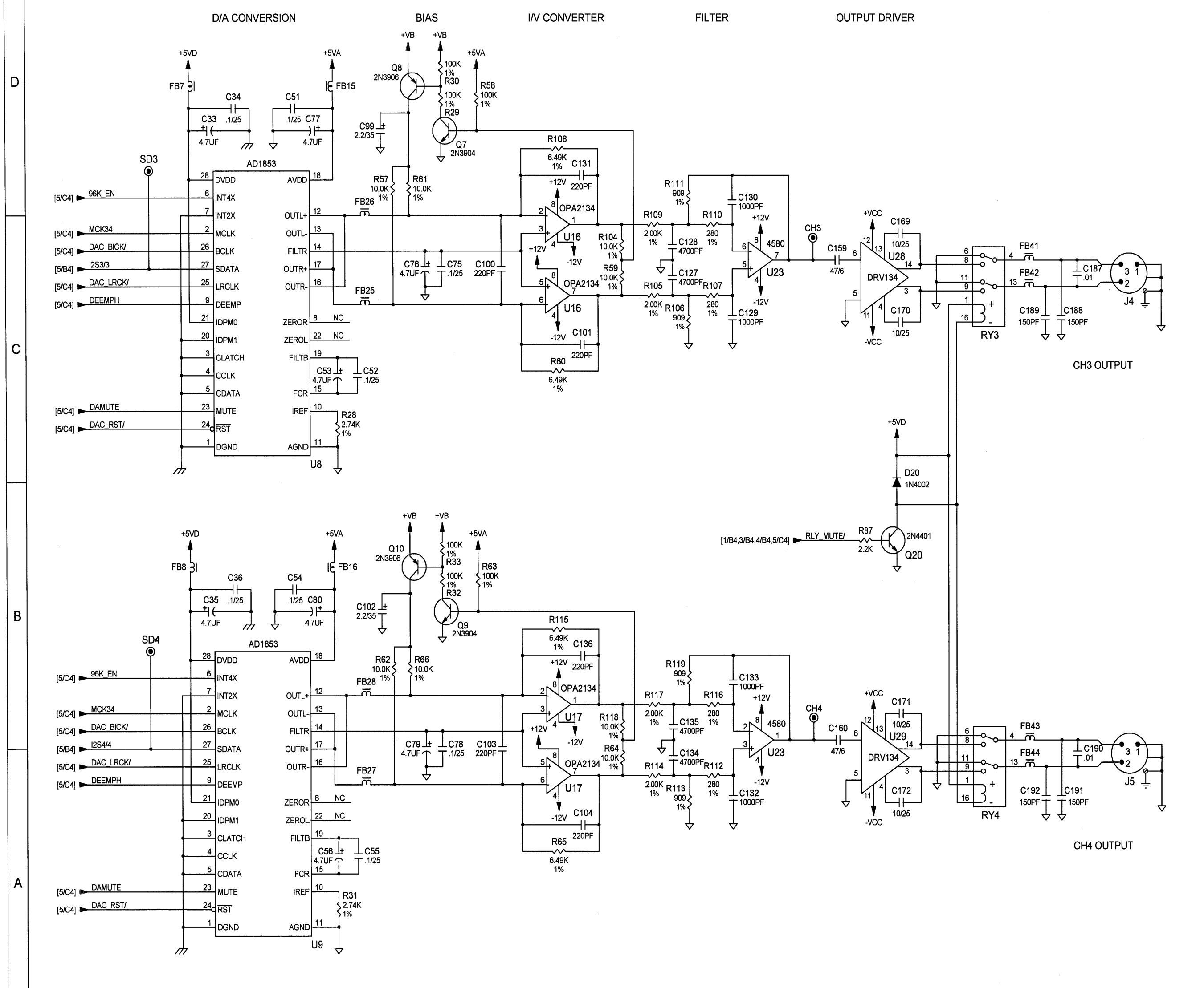
TITLE: SCHEM, AIN BD, 960L POWER

SIZE	CODE	NUMBER	REV
B		060-13339	2

FILE NAME 13339-2.7 SHEET 7 OF 7

1-14-2000_12:54


D/A CONVERSION
BIAS
I/V CONVERTER
FILTER
OUTPUT DRIVER
CH1 OUTPUT
CH2 OUTPUT
NOTES
DOCUMENT CONTROL BLOCK #060-13349
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AOUT BD, 960L
OUTPUT D/A & AMP - CH1 CH2
060-13349



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991201-01	RWH 12/6/99	CW 1/4/00
		ECM 12/29/99	PJM 1/4/00
2	CHANGED PER ECO 000110-00	RWH 1/13/00	CW 1/14/00
		ECM 1/13/00	PJM 1/14/00

CONTRACT NO.

Lexicon
3 OAK PARK
BEDFORD, MA 01730

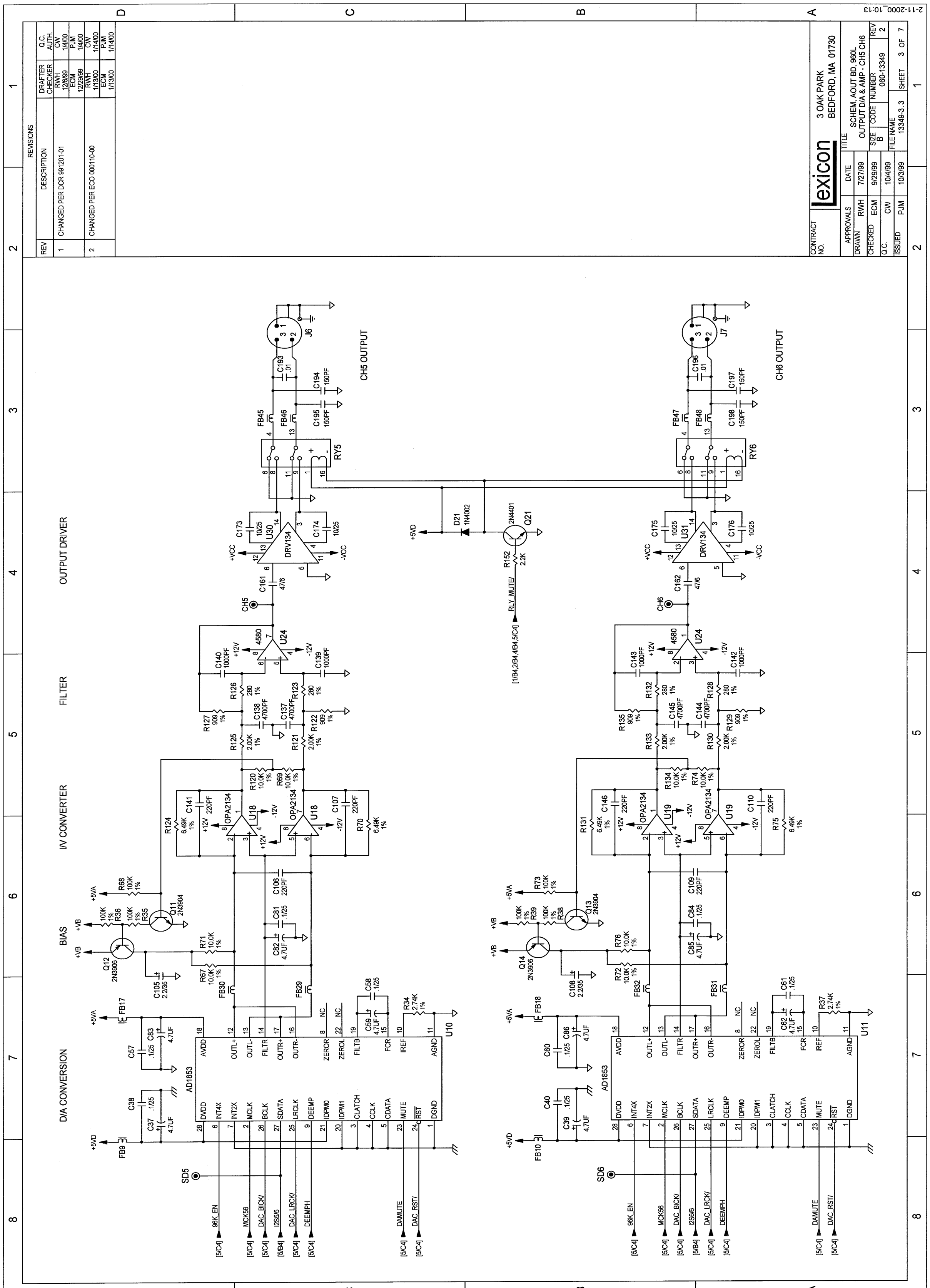
APPROVALS		DATE
DRAWN	RWH	7/27/99
CHECKED	ECM	9/29/99
Q.C.	CW	10/4/99
ISSUED	PJM	10/3/99

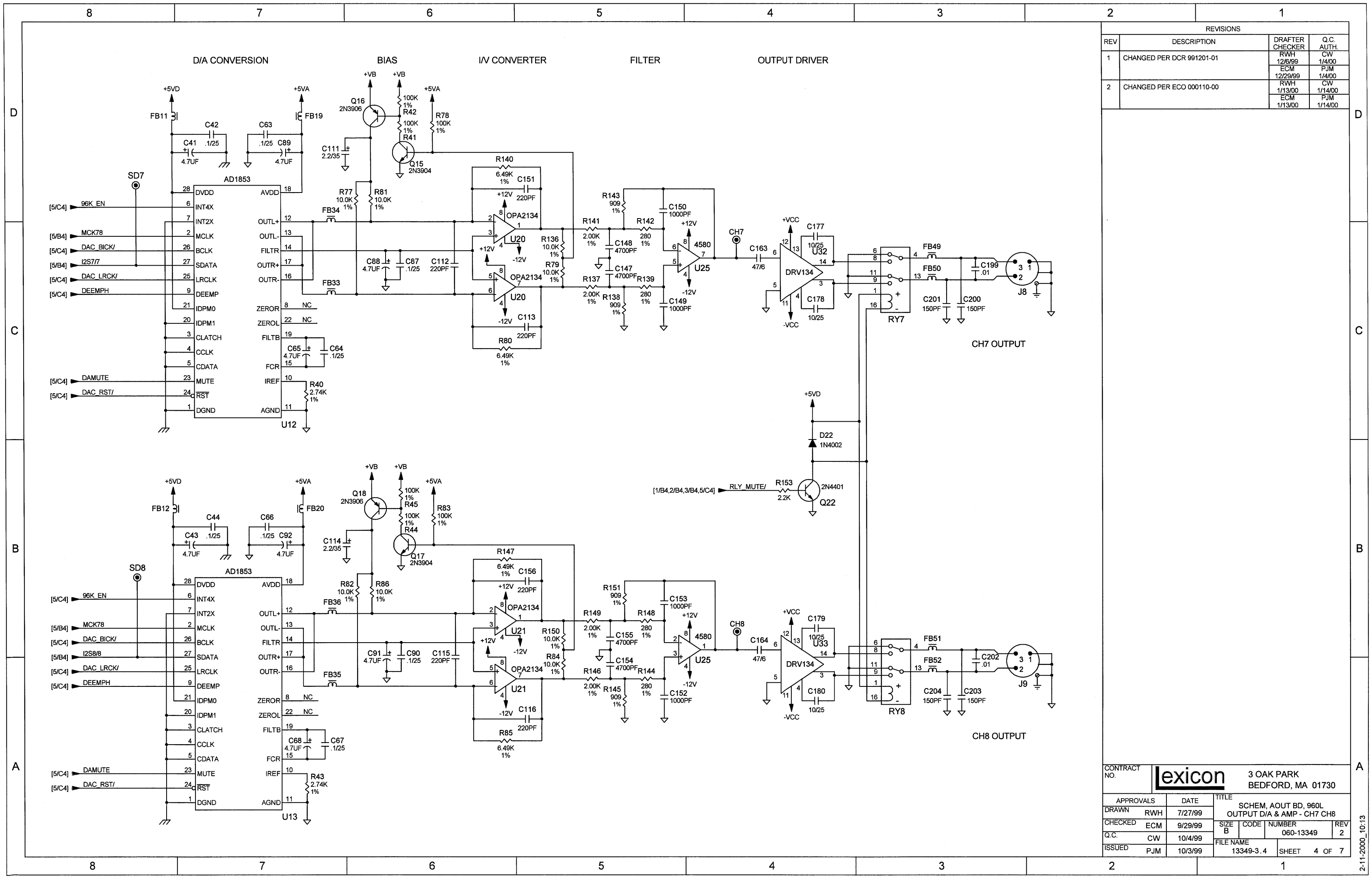
TITLE: SCHEM, AOUT BD, 960L OUTPUT D/A & AMP - CH3 CH4

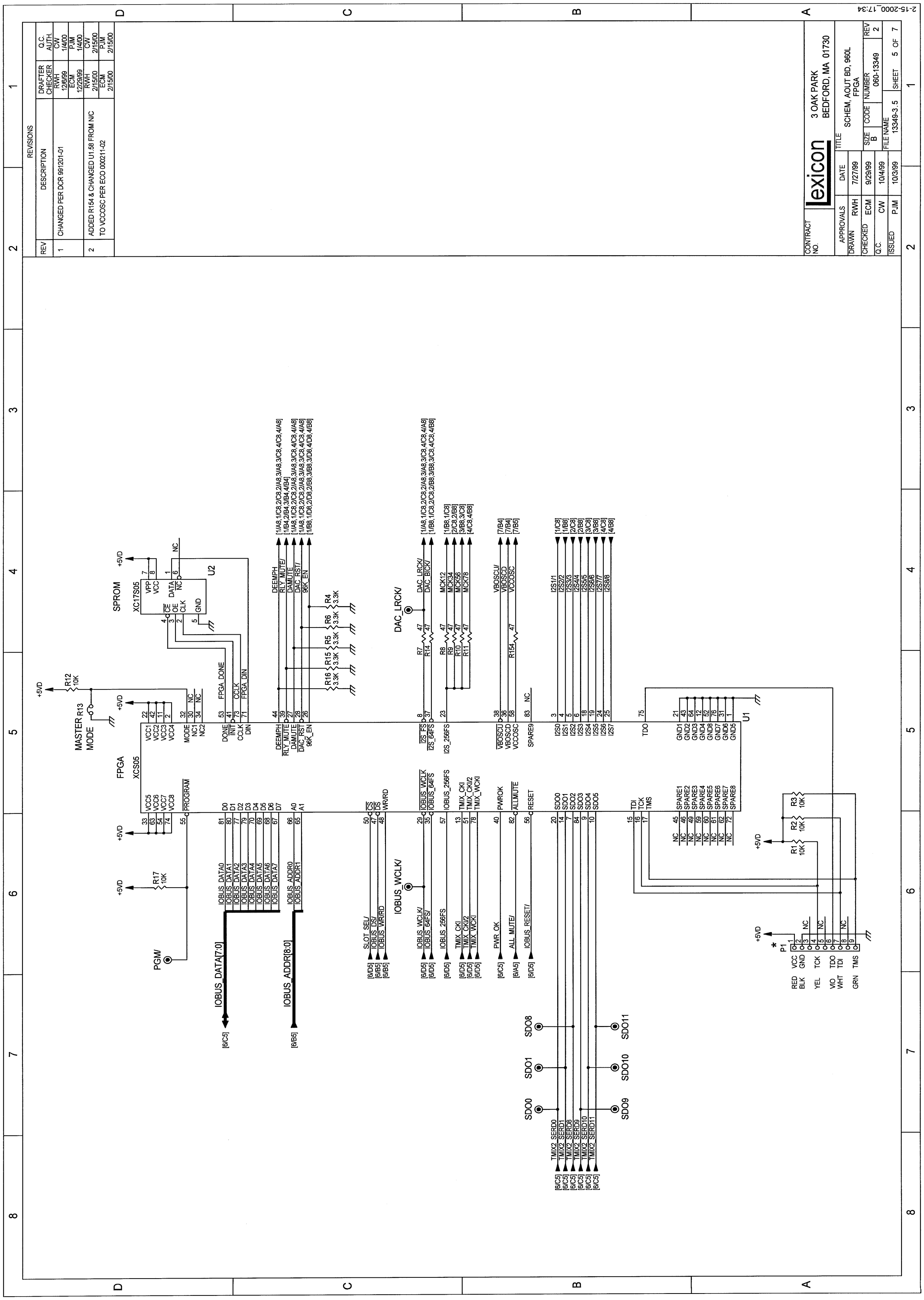
SIZE: B | CODE | NUMBER: 060-13349 | REV: 2

FILE NAME: 13349-3.2 | SHEET 2 OF 7

2-11-2000_10:13

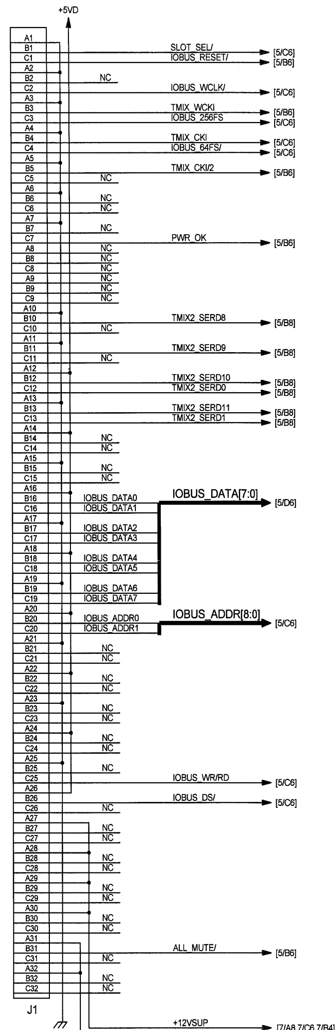

D/A CONVERSION
BIAS
I/V CONVERTER
FILTER
OUTPUT DRIVER
CH5 OUTPUT
CH6 OUTPUT
REVISIONS
CHANGED PER DCR 991201-01
CHANGED PER ECO 000110-00
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AOUT BD, 960L
OUTPUT D/A & AMP - CH5 CH6
060-13349
13349-3.3
SHEET 3 OF 7


D/A CONVERSION
BIAS
I/V CONVERTER
FILTER
OUTPUT DRIVER
CH7 OUTPUT
CH8 OUTPUT
REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991201-01 | RWH 12/6/99 ECM 12/29/99 | CW 1/4/00 PJM 1/4/00
2 | CHANGED PER ECO 000110-00 | RWH 1/13/00 ECM 1/13/00 | CW 1/14/00 PJM 1/14/00
CONTRACT NO.
Lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS | DATE
DRAWN RWH 7/27/99
CHECKED ECM 9/29/99
Q.C. CW 10/4/99
ISSUED PJM 10/3/99
TITLE SCHEM, AOUT BD, 960L OUTPUT D/A & AMP - CH7 CH8
SIZE B
CODE
NUMBER 060-13349
REV 2
FILE NAME 13349-3.4
SHEET 4 OF 7
2-11-2000_10:13


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AOUT BD, 960L
FPGA
060-13349
13349-3.5
SHEET 5 OF 7

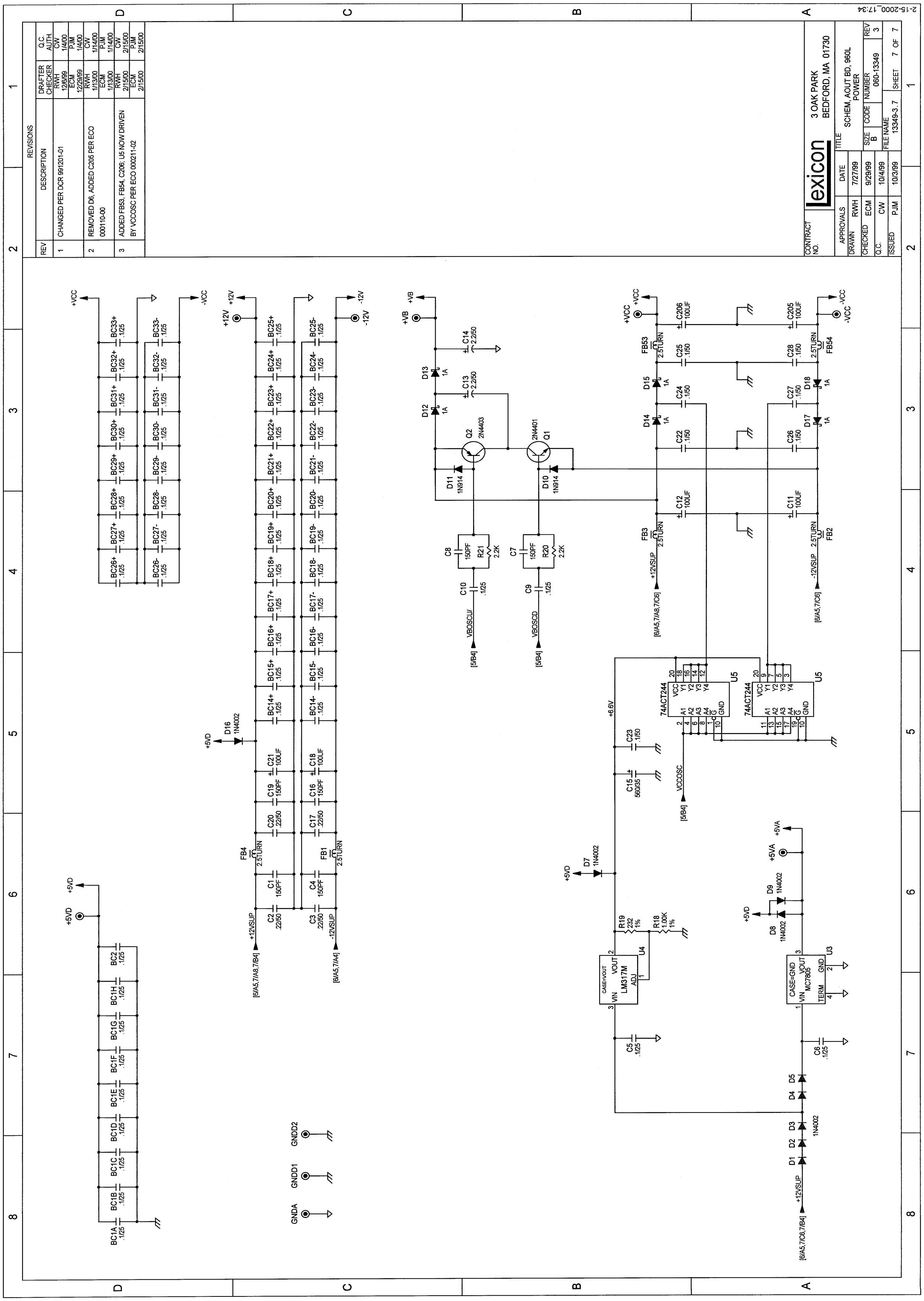
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991201-01	RWH 12/6/99	CW 1/4/00
		ECM 12/29/99	PJM 1/4/00

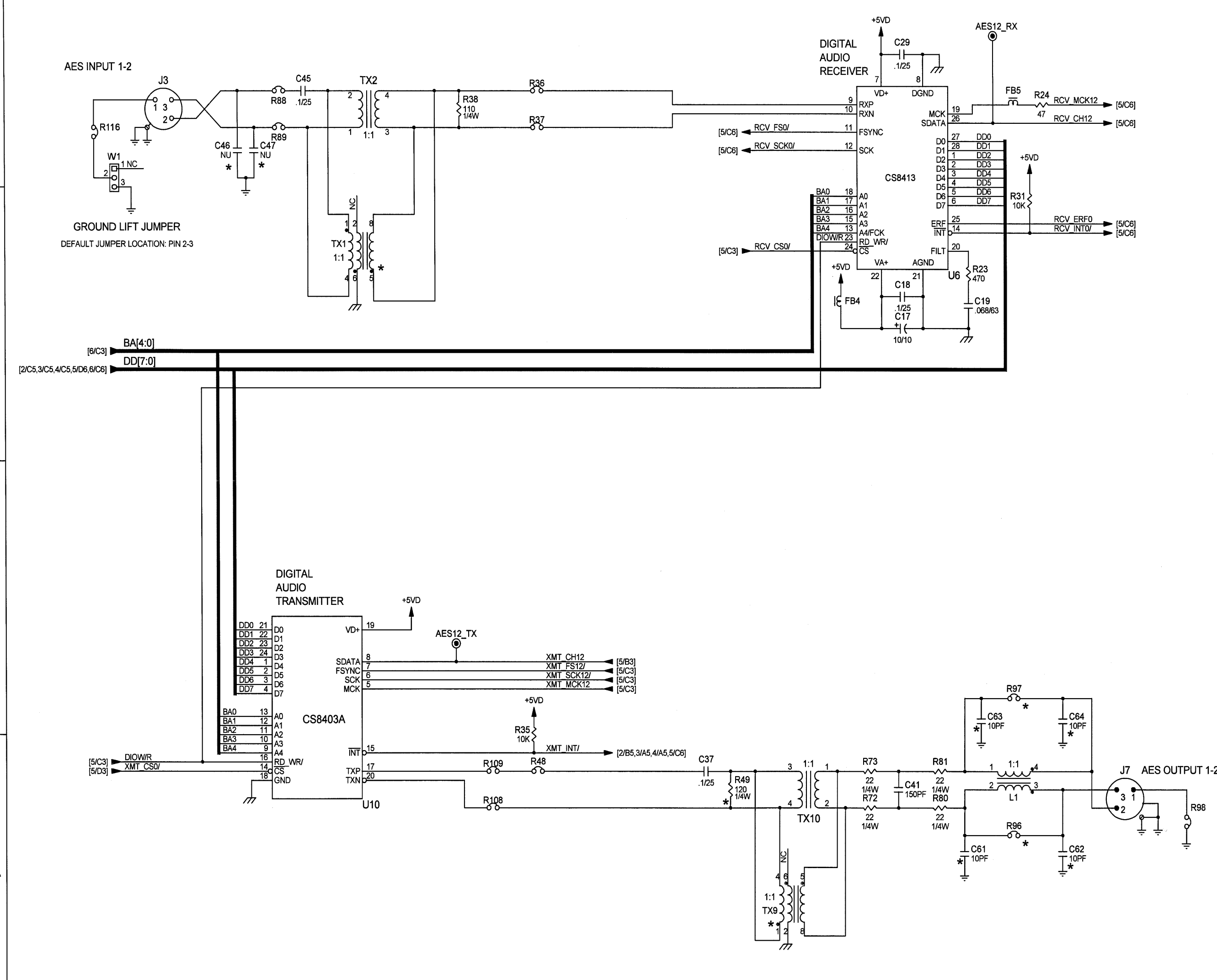
ROW A	ROW B	ROW C
GROUND	SLOT_SEL/	IOBUS_RESET/
GROUND	IOBUS_128FS	IOBUS_WCLK/
GROUND	TMIX_WCKI	IOBUS_256FS
GROUND	TMIX_CKI	IOBUS_64FS/
GROUND	TMIX_CKI/2	SLOT_WCLK/
GROUND	SLOT_PCLK_INT/	BSPARE1
GROUND	ASPARE9	PWR_OK
BSPARE2	TMIX1_SERD10	TMIX1_SERD0
ASPARE1	TMIX1_SERD11	TMIX1_SERD1
GROUND	TMIX2_SERD8	TMIX1_SERD2
GROUND	TMIX2_SERD9	TMIX1_SERD3
+5V	TMIX2_SERD10	TMIX2_SERD0
GROUND	TMIX2_SERD11	TMIX2_SERD1
+5V	ASPARE2	TMIX2_SERD2
GROUND	TMIX2_SERD3	ASPARE3
+5V	IOBUS_DATA0	IOBUS_DATA1
GROUND	IOBUS_DATA2	IOBUS_DATA3
+5V	IOBUS_DATA4	IOBUS_DATA5
GROUND	IOBUS_DATA6	IOBUS_DATA7
+5V	IOBUS_ADDR0	IOBUS_ADDR1
GROUND	IOBUS_ADDR2	IOBUS_ADDR3
+5V	IOBUS_ADDR4	IOBUS_ADDR5
GROUND	IOBUS_ADDR6	IOBUS_ADDR7
+5V	IOBUS_ADDR8	IOBUS_RD/
GROUND	IOBUS_INT/	IOBUS_WR/RD
+5V	IOBUS_DS/	MIDI_TX
+12V	IOBUS_AS/	MIDI_RX
+12V	ASPARE4	ASPARE5
+12V	RS232TX2	RS232TX1
+12V	RS232RX2	RS232RX1
-12V	IOBUS_ALLMUTE/	ASPARE6
-12V	ASPARE7	ASPARE8



CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730
APPROVALS	DATE	TITLE SCHEM, AOUT BD, 960L BACKPLANE INTERFACE
DRAWN RWH	7/27/99	
CHECKED ECM	9/29/99	SIZE B, CODE, NUMBER 060-13349, REV 1
Q.C. CW	10/4/99	FILE NAME 13349-3.6
ISSUED PJM	10/3/99	SHEET 6 OF 7

2-11-2000_12:07


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, AOUT BD, 960L
POWER
060-13349



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991130-00	RWH 1/4/00	CW 1/4/00
		JV 1/4/00	PJM 1/5/00
2	CHANGED COMPONENTS / VALUES & SHEETS 2-4 PER ECO 000320-00	RWH 4/6/00	CW 4/17/00
		JV 4/16/00	PJM 4/27/00
3	RENUMBERED SHTS 1-4 PER ECO 000320-00	RWH 6/5/00	CW 6/6/00
		JV 6/6/00	JW 6/6/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND, ANALOG GROUND, CHASSIS GROUND, POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 COMPONENTS MARKED WITH * ARE NOT INSTALLED

7 LAST REFERENCE DESIGNATORS USED: C76, D1, FB11, J10, L4, R119, TX16, U13, W4.

DOCUMENT CONTROL BLOCK: #060-13359

SHEET NUMBER	REVISION NUMBER
1 OF 8	3
2 OF 8	3
3 OF 8	3
4 OF 8	3
5 OF 8	1
6 OF 8	1
7 OF 8	1
8 OF 8	1

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

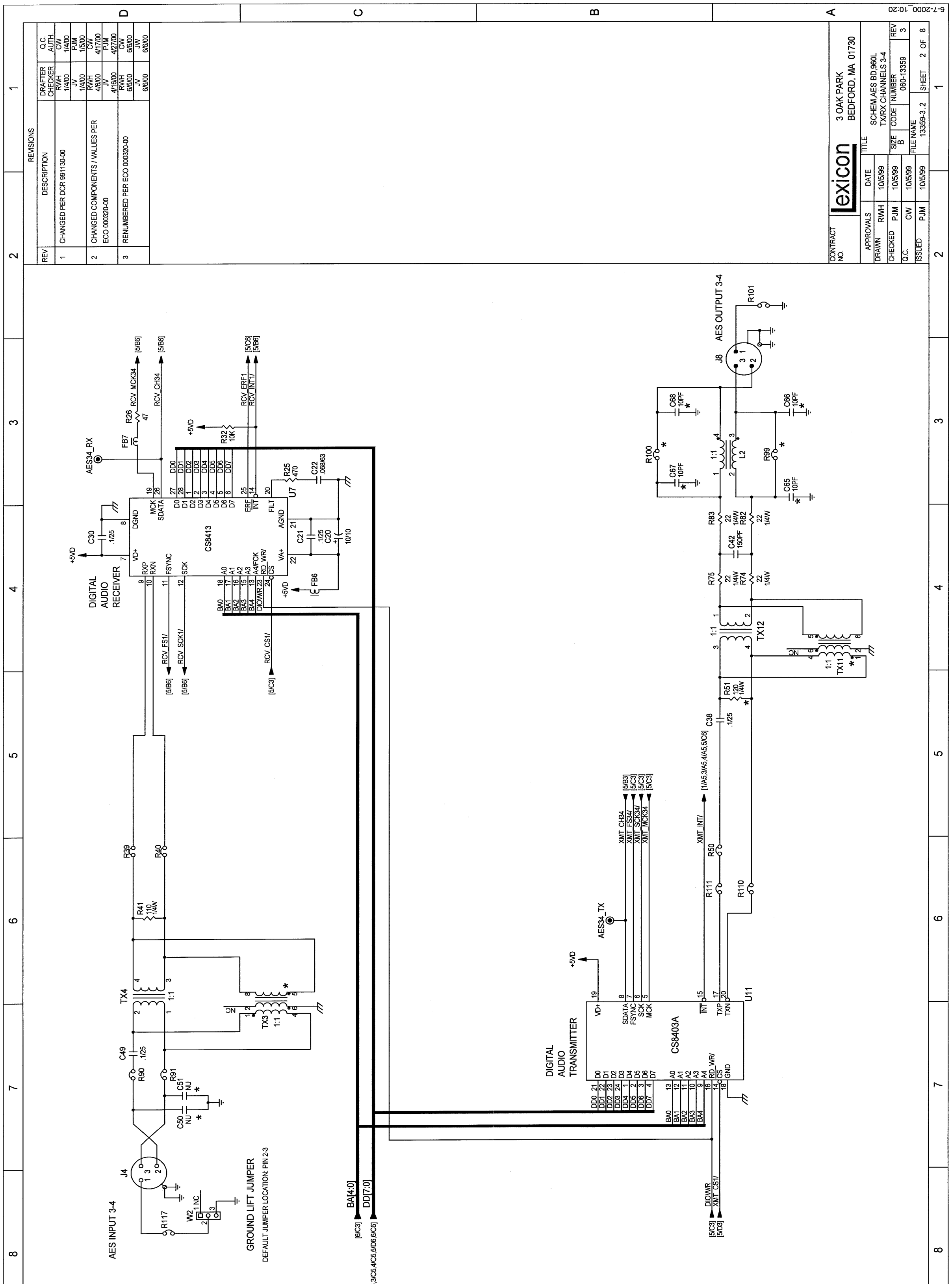
APPROVALS		DATE
DRAWN	RWH	10/5/99
CHECKED	PJM	10/5/99
Q.C.	CW	10/5/99
ISSUED	PJM	10/5/99

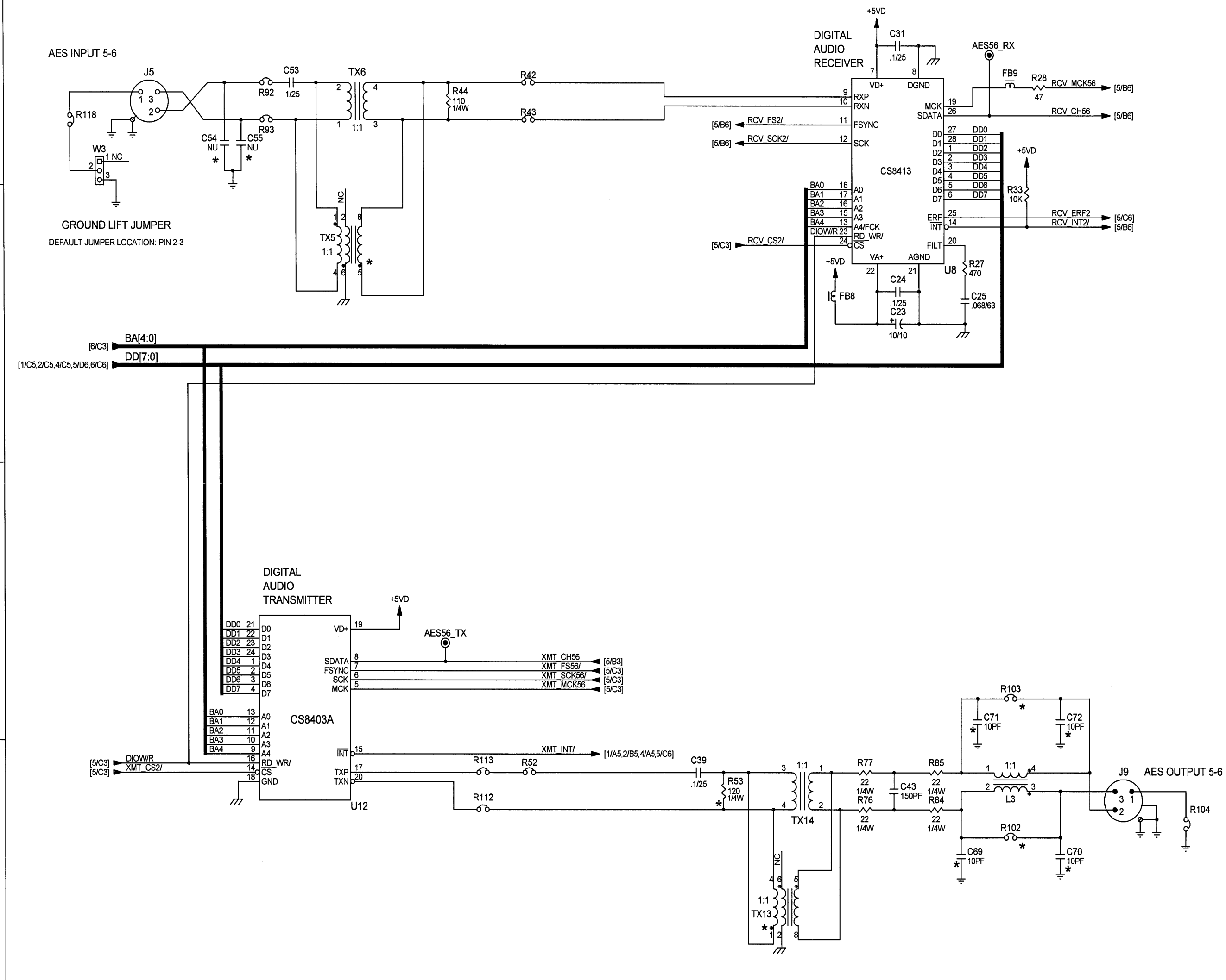
TITLE SCHEM,AES BD,960L TX/RX CHANNELS 1-2

SIZE B | CODE | NUMBER 060-13359 | REV 3

FILE NAME 13359-3.1 | SHEET 1 OF 8

6-7-2000_10:20


AES INPUT 3-4
GROUND LIFT JUMPER
DEFAULT JUMPER LOCATION: PIN 2-3
DIGITAL AUDIO RECEIVER
CS8413
DIGITAL AUDIO TRANSMITTER
CS8403A
AES OUTPUT 3-4
3 OAK PARK
BEDFORD, MA 01730
SCHEM,AES BD,960L
TX/RX CHANNELS 3-4
060-13359
13359-3_2
SHEET 2 OF 8



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991130-00	RWH 1/4/00 JV 1/4/00	CW 1/4/00 PJM 1/5/00
2	CHANGED COMPONENTS / VALUES PER ECO 000320-00	RWH 4/6/00 JV 4/16/00	CW 4/17/00 PJM 4/27/00
3	RENUMBERED PER ECO 000320-00	RWH 6/5/00 JV 6/6/00	CW 6/6/00 JW 6/6/00

CONTRACT NO.

Lexicon

3 OAK PARK
BEDFORD, MA 01730

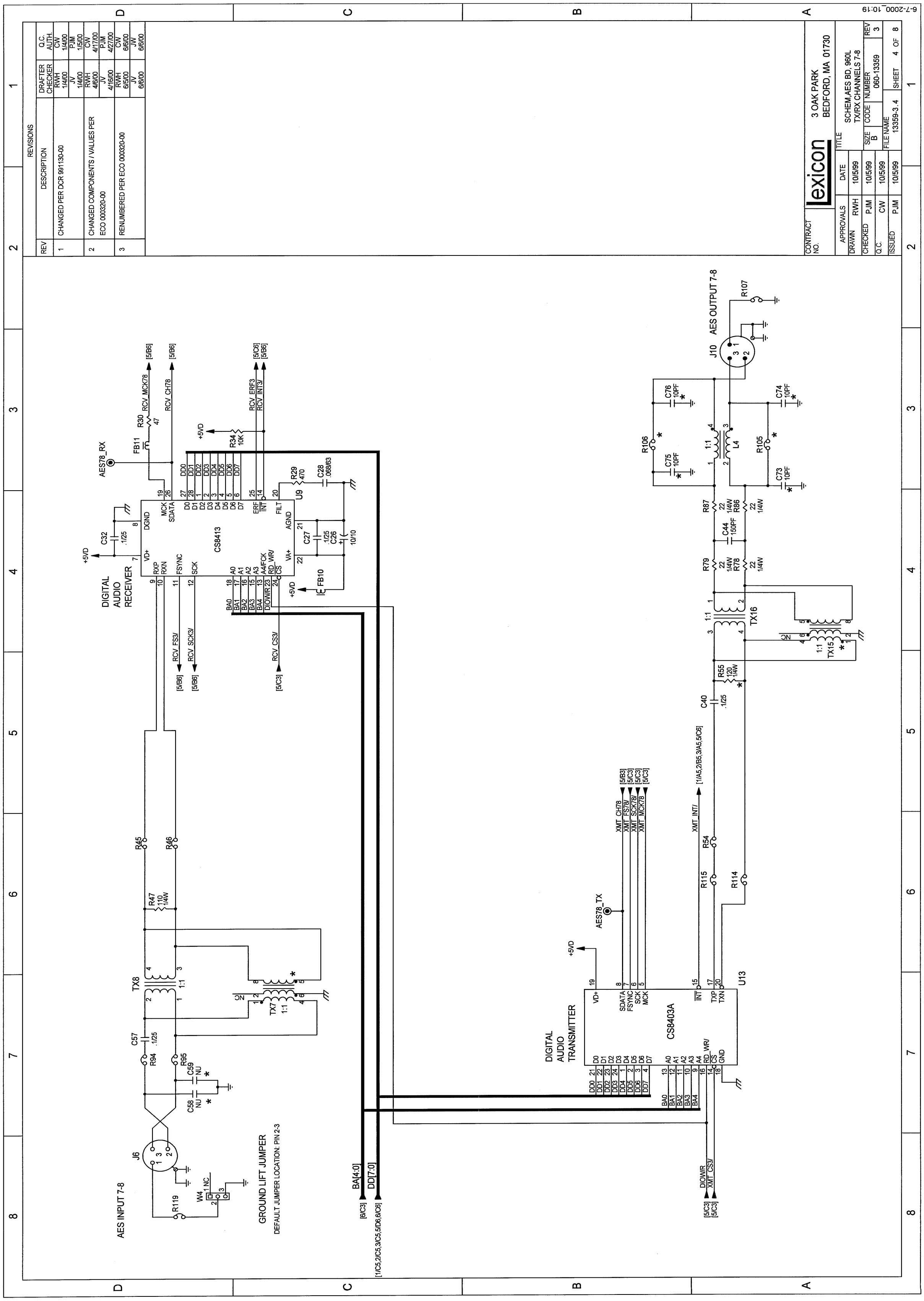
APPROVALS		DATE
DRAWN	RWH	10/5/99
CHECKED	PJM	10/5/99
Q.C.	CW	10/5/99
ISSUED	PJM	10/5/99

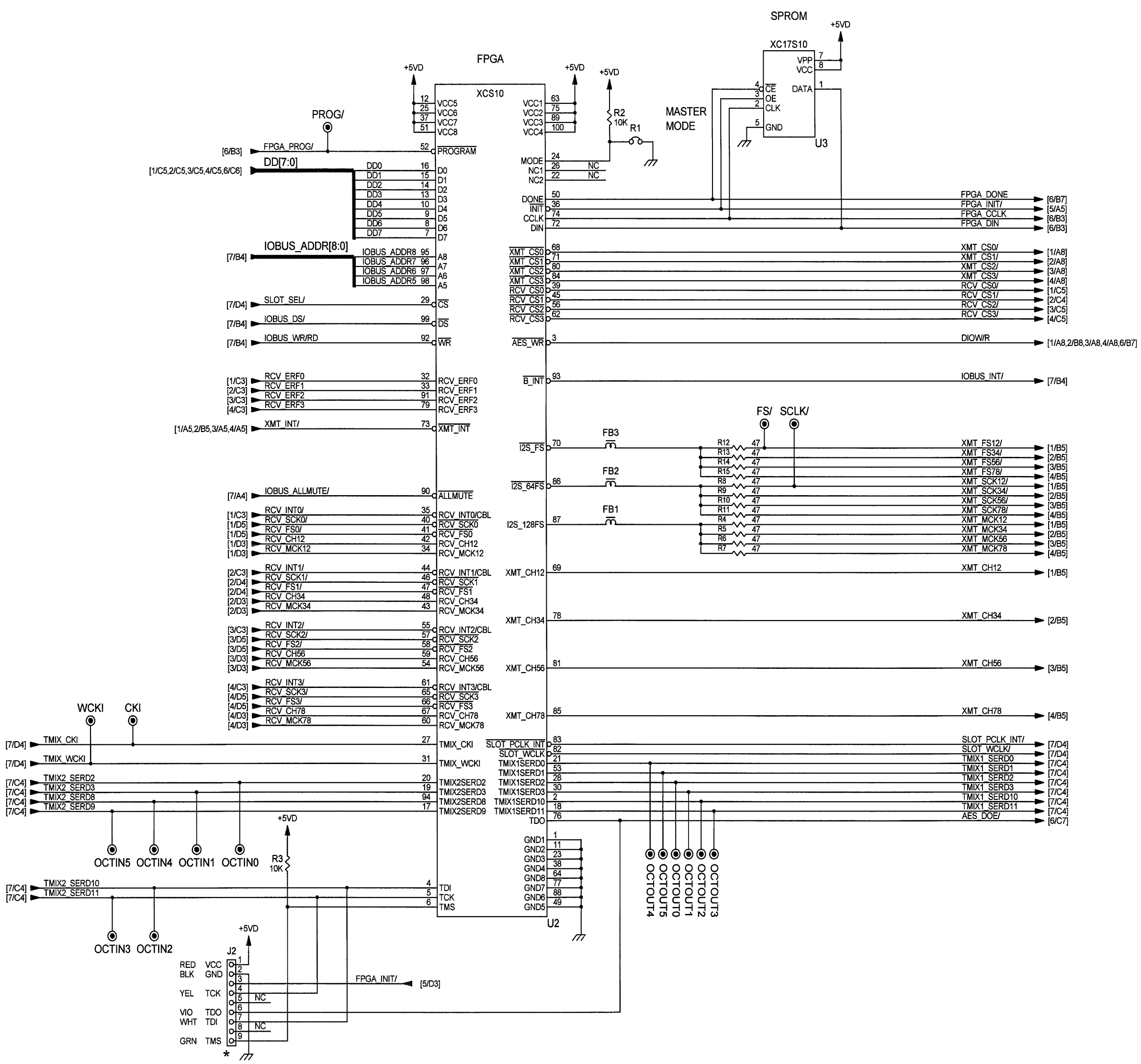
TITLE SCHEM,AES BD, 960L TX/RX CHANNELS 5-6

SIZE B | CODE | NUMBER 060-13359 | REV 3

FILE NAME 13359-3.3 | SHEET 3 OF 8

6-7-2000_10:19

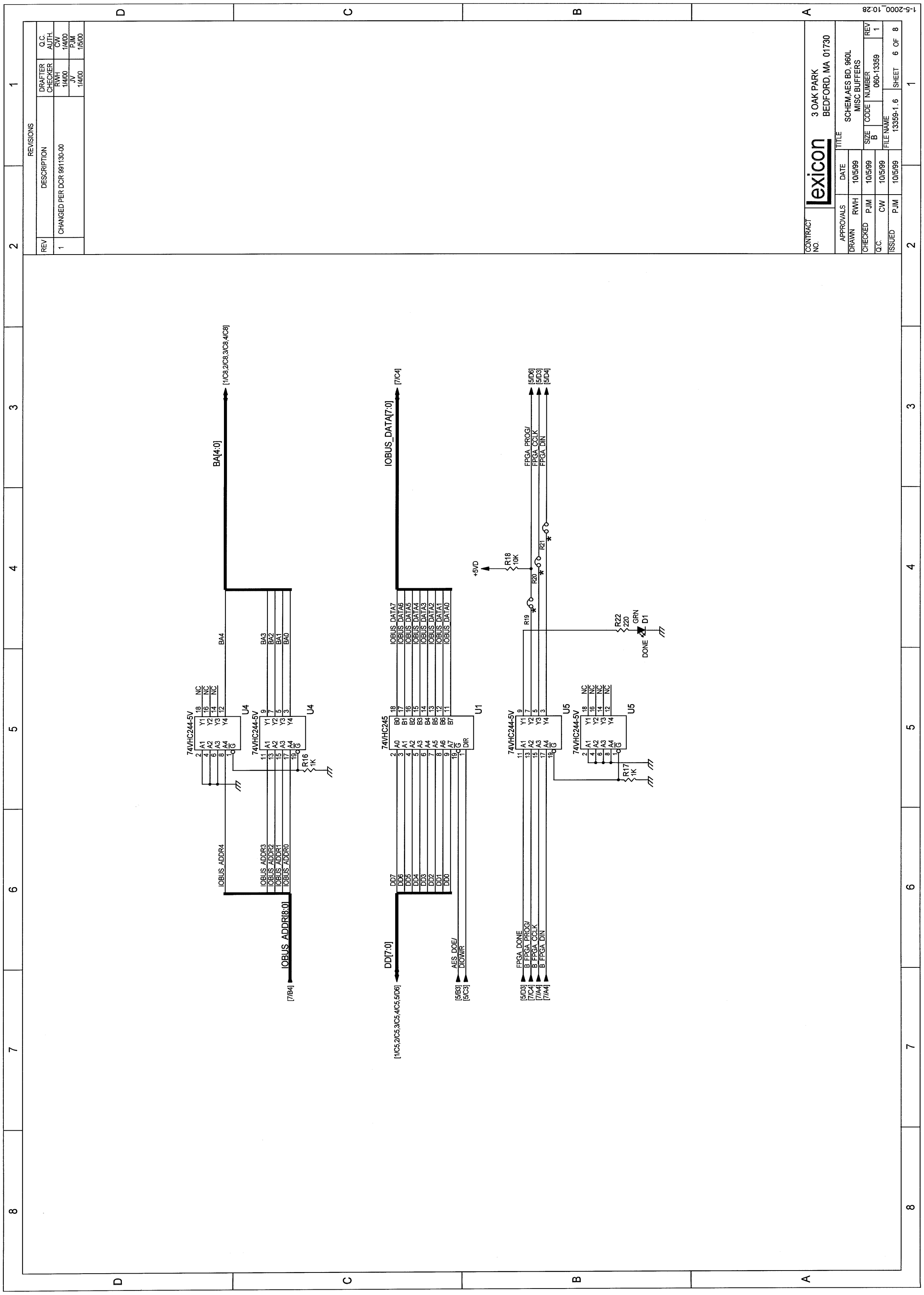

REVISIONS
CHANGED PER DCR 991130-00
CHANGED COMPONENTS / VALUES PER ECO 000320-00
RENUMBERED PER ECO 000320-00
DIGITAL AUDIO RECEIVER
CS8413
DIGITAL AUDIO TRANSMITTER
CS8403A
AES INPUT 7-8
AES OUTPUT 7-8
GROUND LIFT JUMPER
DEFAULT JUMPER LOCATION: PIN 2-3
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,AES BD, 960L
TX/RX CHANNELS 7-8
060-13359
13359-3.4
SHEET 4 OF 8
6-7-2000_10:19



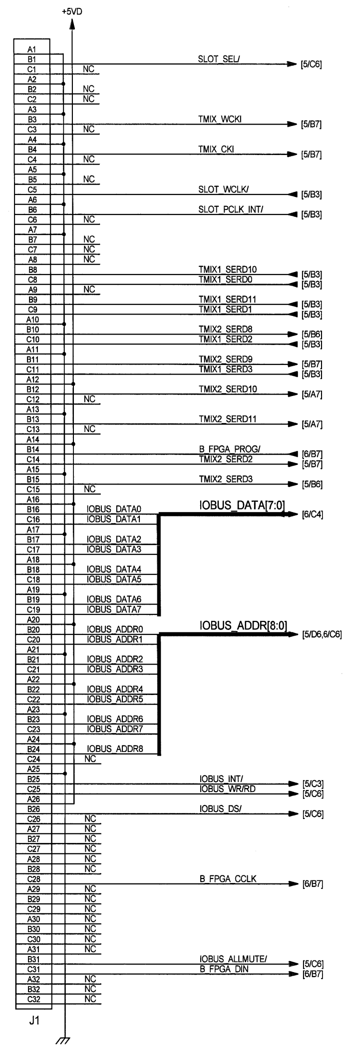
REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991130-00	RWH 1/4/00 JV 1/4/00	CW 1/4/00 PJM 1/5/00

CONTRACT NO.	lexicon	3 OAK PARK BEDFORD, MA 01730	
APPROVALS		DATE	TITLE SCHEM,AES BD, 960L AUDIO & CONTROL FPGA
DRAWN	RWH	10/5/99	
CHECKED	PJM	10/5/99	SIZE B · CODE · NUMBER 060-13359 · REV 1
Q.C.	CW	10/5/99	FILE NAME 13359-1.5
ISSUED	PJM	10/5/99	SHEET 5 OF 8

1-5-2000_10:31


BA[4:0]
IOBUS_DATA[7:0]
IOBUS_ADDR[8:0]
DD[7:0]
74VHC244-5V
74VHC245
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM,AES BD, 960L
MISC BUFFERS
060-13359
13359-1.6
6 OF 8

	ROW	
A	B	C
GROUND	SLOT_SEL/	IOBUS_RESET/
GROUND	IOBUS_128FS	IOBUS_WCLK/
GROUND	TMIX_WCKI	IOBUS_256FS
GROUND	TMIX_CKI	IOBUS_64FS/
GROUND	TMIX_CKI/2	SLOT_WCLK/
GROUND	SLOT_PCLK_INT/	BSPARE1
GROUND	ASPARE9	PWR_OK
BSPARE2	TMIX1_SERD10	TMIX1_SERD0
ASPARE1	TMIX1_SERD11	TMIX1_SERD1
GROUND	TMIX2_SERD8	TMIX1_SERD2
GROUND	TMIX2_SERD9	TMIX1_SERD3
+5V	TMIX2_SERD10	TMIX2_SERD0
GROUND	TMIX2_SERD11	TMIX2_SERD1
+5V	ASPARE2	TMIX2_SERD2
GROUND	TMIX2_SERD3	ASPARE3
+5V	IOBUS_DATA0	IOBUS_DATA1
GROUND	IOBUS_DATA2	IOBUS_DATA3
+5V	IOBUS_DATA4	IOBUS_DATA5
GROUND	IOBUS_DATA6	IOBUS_DATA7
+5V	IOBUS_ADDR0	IOBUS_ADDR1
GROUND	IOBUS_ADDR2	IOBUS_ADDR3
+5V	IOBUS_ADDR4	IOBUS_ADDR5
GROUND	IOBUS_ADDR6	IOBUS_ADDR7
+5V	IOBUS_ADDR8	IOBUS_RD/
GROUND	IOBUS_INT/	IOBUS_WR/RD
+5V	IOBUS_DS/	MIDI_TX
+12V	IOBUS_AS/	MIDI_RX
+12V	ASPARE4	ASPARE5
+12V	RS232TX2	RS232TX1
+12V	RS232RX2	RS232RX1
-12V	IOBUS_ALLMUTE/	ASPARE6
-12V	ASPARE7	ASPARE8



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991130-00	RWH 1/4/00 JV 1/4/00	CW 1/4/00 PJM 1/5/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

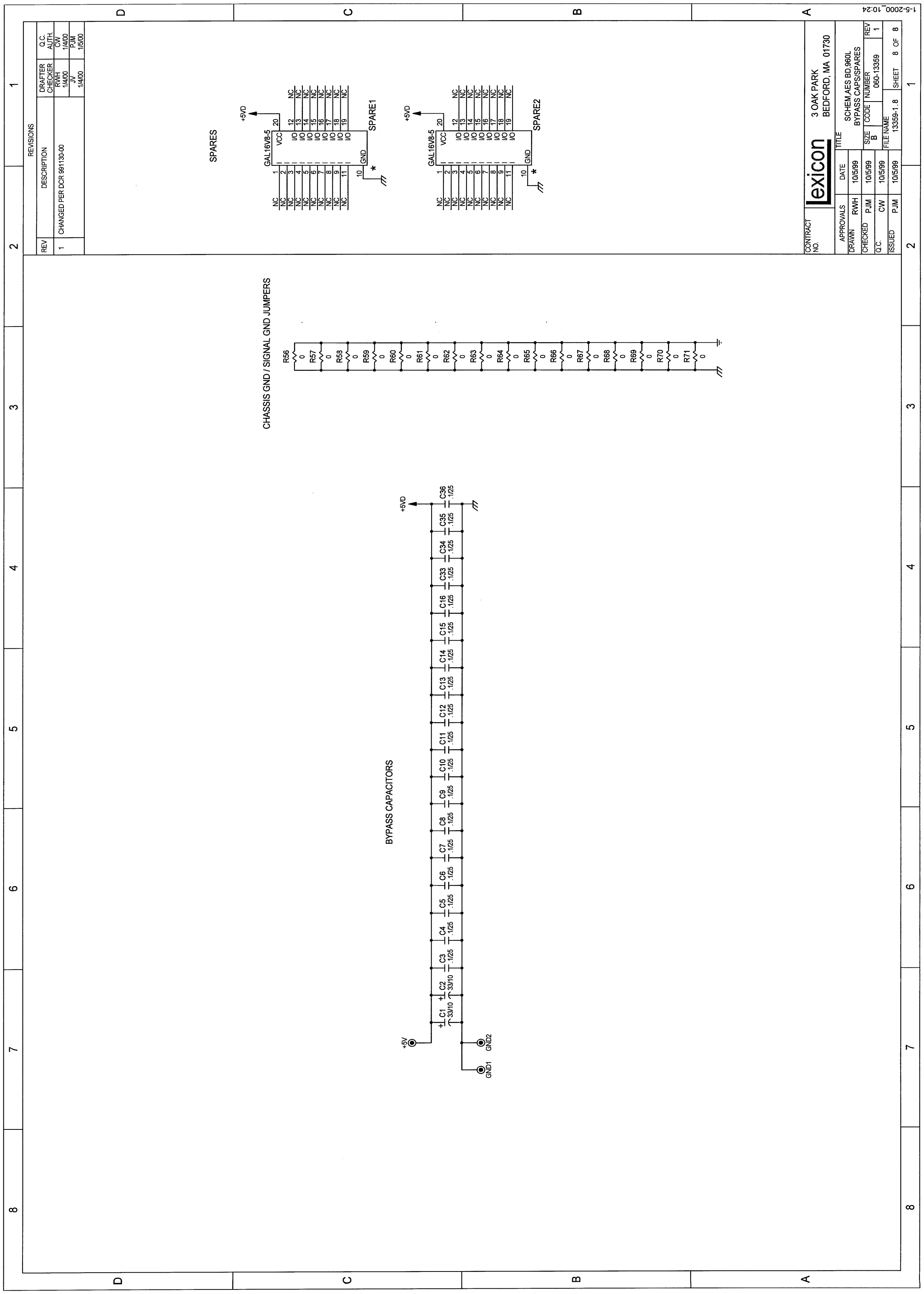
APPROVALS		DATE
DRAWN	RWH	10/5/99
CHECKED	PJM	10/5/99
Q.C.	CW	10/5/99
ISSUED	PJM	10/5/99

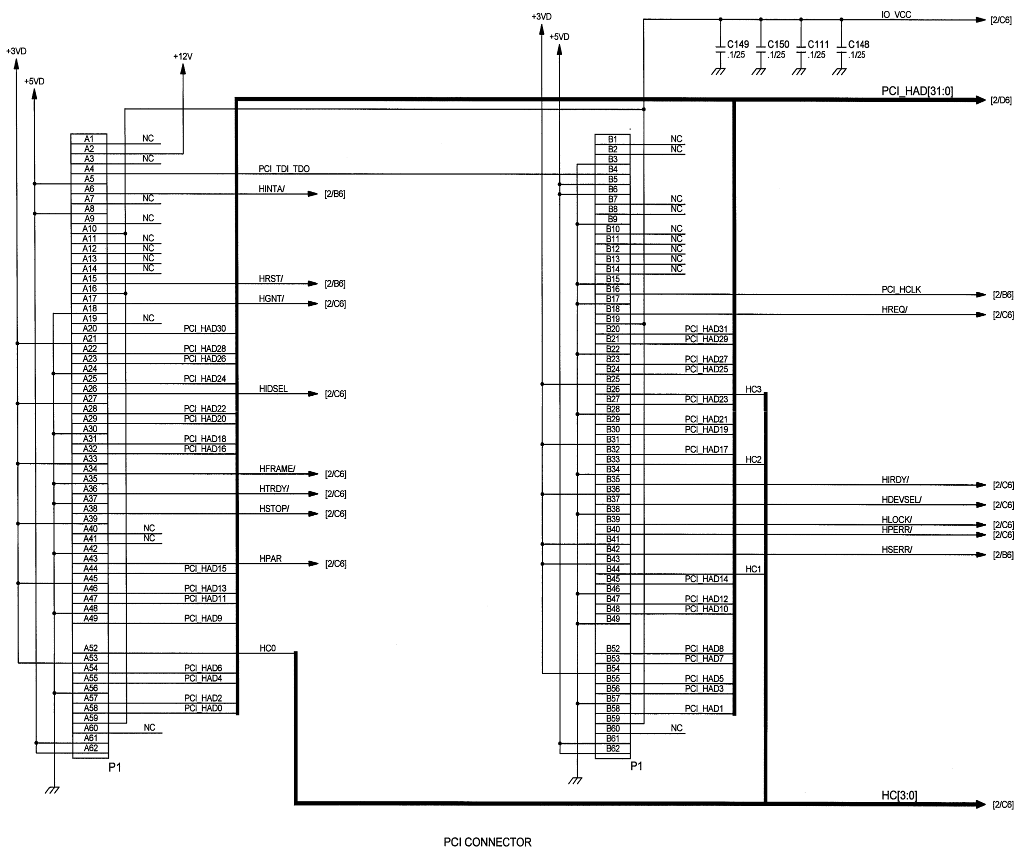
TITLE SCHEM,AES BD, 960L IO BACKPLANE CONNECTOR

SIZE B | CODE | NUMBER 060-13359 | REV 1

FILE NAME 13359-1.7 | SHEET 7 OF 8

1-5-2000_10:22


REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH
1
CHANGED PER DCR 991130-00
RWH 1/4/00
CW 1/4/00
JV 1/4/00
PJM 1/5/00
SPARES
GAL16V8-5
SPARE1
SPARE2
+5VD
CHASSIS GND / SIGNAL GND JUMPERS
BYPASS CAPACITORS
+5V
GND1
GND2
CONTRACT NO.
APPROVALS
DATE
DRAWN RWH 10/5/99
CHECKED PJM 10/5/99
Q.C. CW 10/5/99
ISSUED PJM 10/5/99
lexicon
3 OAK PARK
BEDFORD, MA 01730
TITLE
SCHEM,AES BD,960L
BYPASS CAPS/SPARES
SIZE B
CODE
NUMBER 060-13359
REV 1
FILE NAME 13359-1.8
SHEET 8 OF 8
1-5-2000_10:24



PCI CONNECTOR

REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991029-01	RWH 10/29/99	CW 11/1/99
		JV 11/1/99	JV 11/2/99
2	CHANGED PER DCR 991208-00	RWH 12/29/99	CW 12/30/99
		JV 12/28/99	PJM 1/5/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND; ANALOG GROUND; CHASSIS GROUND; POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6. COMPONENTS MARKED WITH * ARE NOT INSTALLED.

7 LAST REFERENCE DESIGNATORS USED: C152, D10, J2, P2, R196, U50, Y1.

DOCUMENT CONTROL BLOCK: #060-13369

SHEET NUMBER	REVISION NUMBER
1 OF 16	2
2 OF 16	2
3 OF 16	2
4 OF 16	2
5 OF 16	2
6 OF 16	2
7 OF 16	2
8 OF 16	2
9 OF 16	2
10 OF 16	2
11 OF 16	2
12 OF 16	2
13 OF 16	2
14 OF 16	2
15 OF 16	2
16 OF 16	2

CONTRACT NO.

lexicon — 3 OAK PARK, BEDFORD, MA 01730

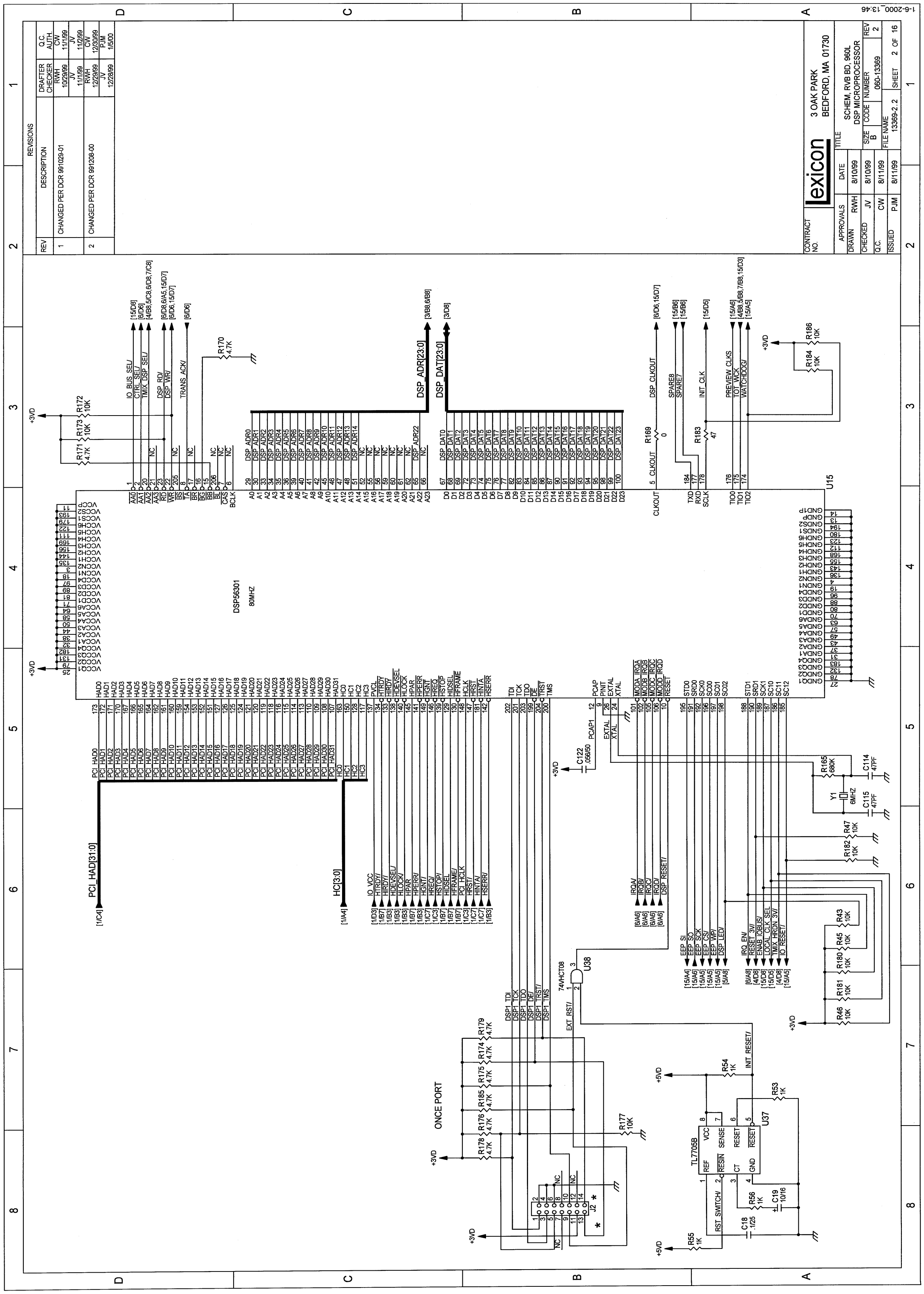
APPROVALS		DATE
DRAWN	RWH	8/10/99
CHECKED	JV	8/10/99
Q.C.	CW	8/11/99
ISSUED	PJM	8/11/99

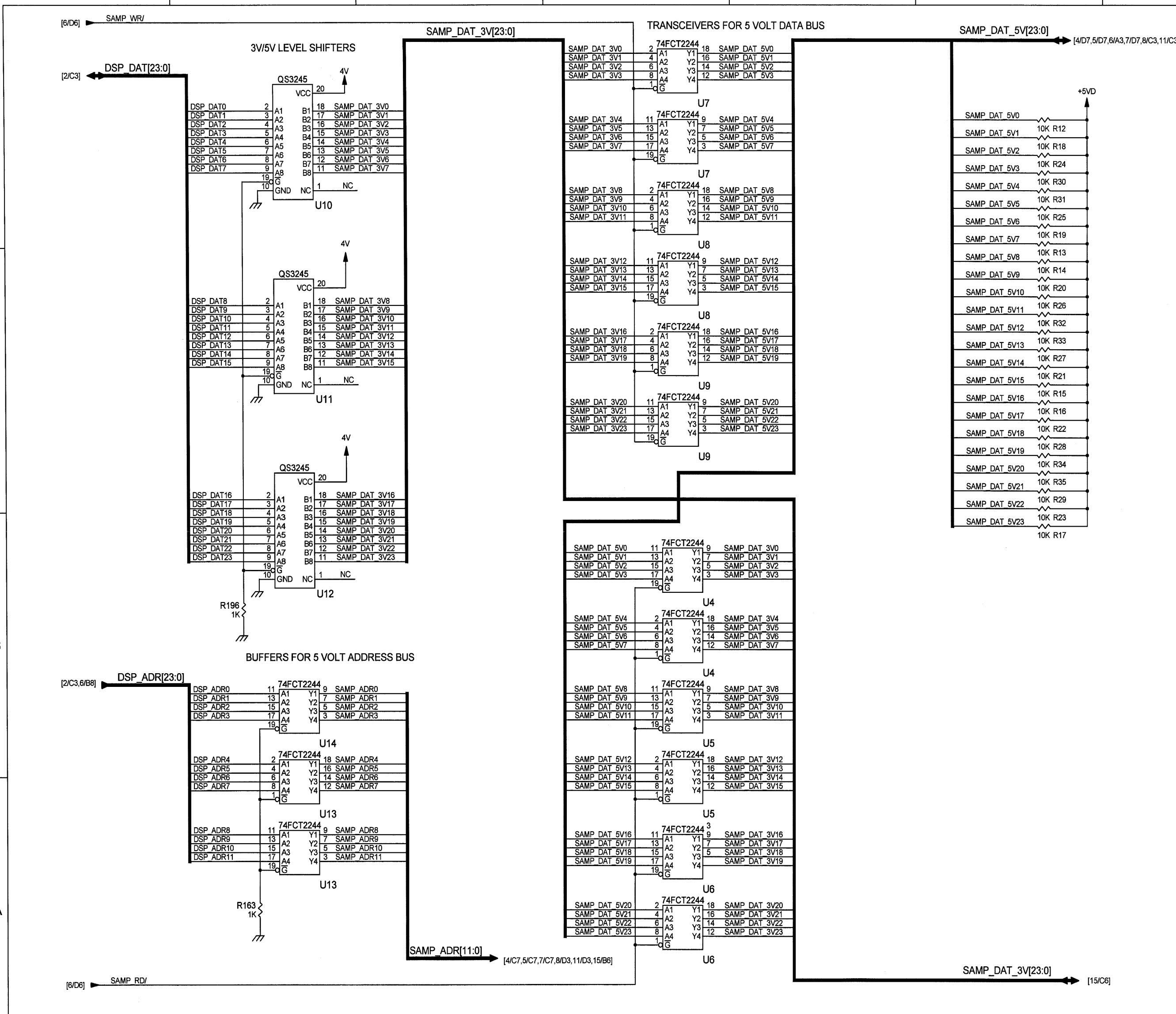
TITLE: SCHEM, RVB BD, 960L PCI CONNECTOR

SIZE: B | CODE: | NUMBER: 060-13369 | REV: 2

FILE NAME: 13369-2.1 | SHEET 1 OF 16

1-6-2000_13:45


3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
DSP MICROPROCESSOR
060-13369
SHEET 2 OF 16
DSP56301
80MHZ
ONCE PORT



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991029-01	RWH 10/29/99 JV 11/1/99	CW 11/1/99 JV 11/2/99
2	CHANGED PER DCR 991208-00	RWH 12/29/99 JV 12/28/99	CW 12/30/99 PJM 1/5/00

CONTRACT NO.

lexicon

3 OAK PARK
BEDFORD, MA 01730

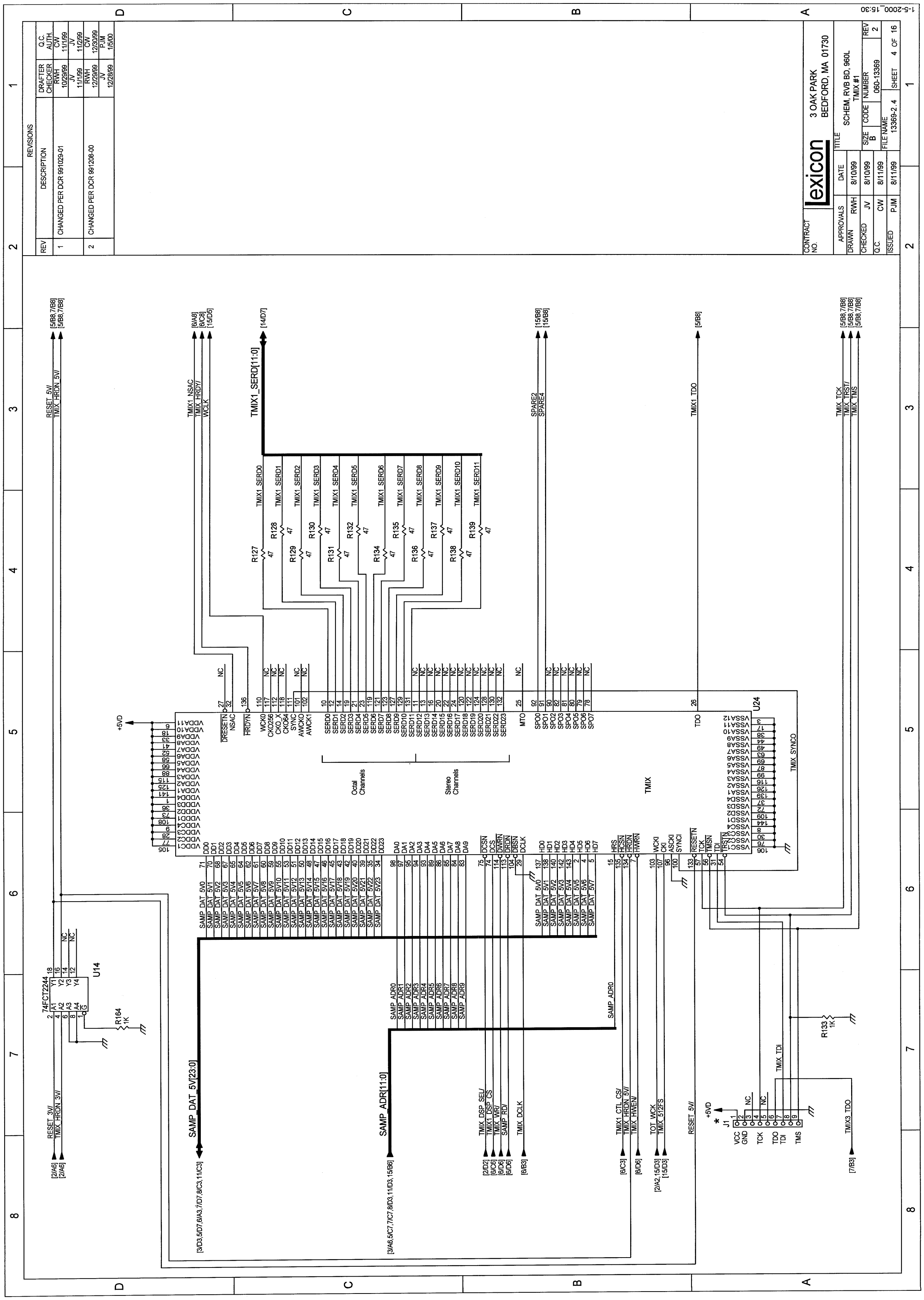
APPROVALS		DATE
DRAWN	RWH	8/10/99
CHECKED	JV	8/10/99
Q.C.	CW	8/11/99
ISSUED	PJM	8/11/99

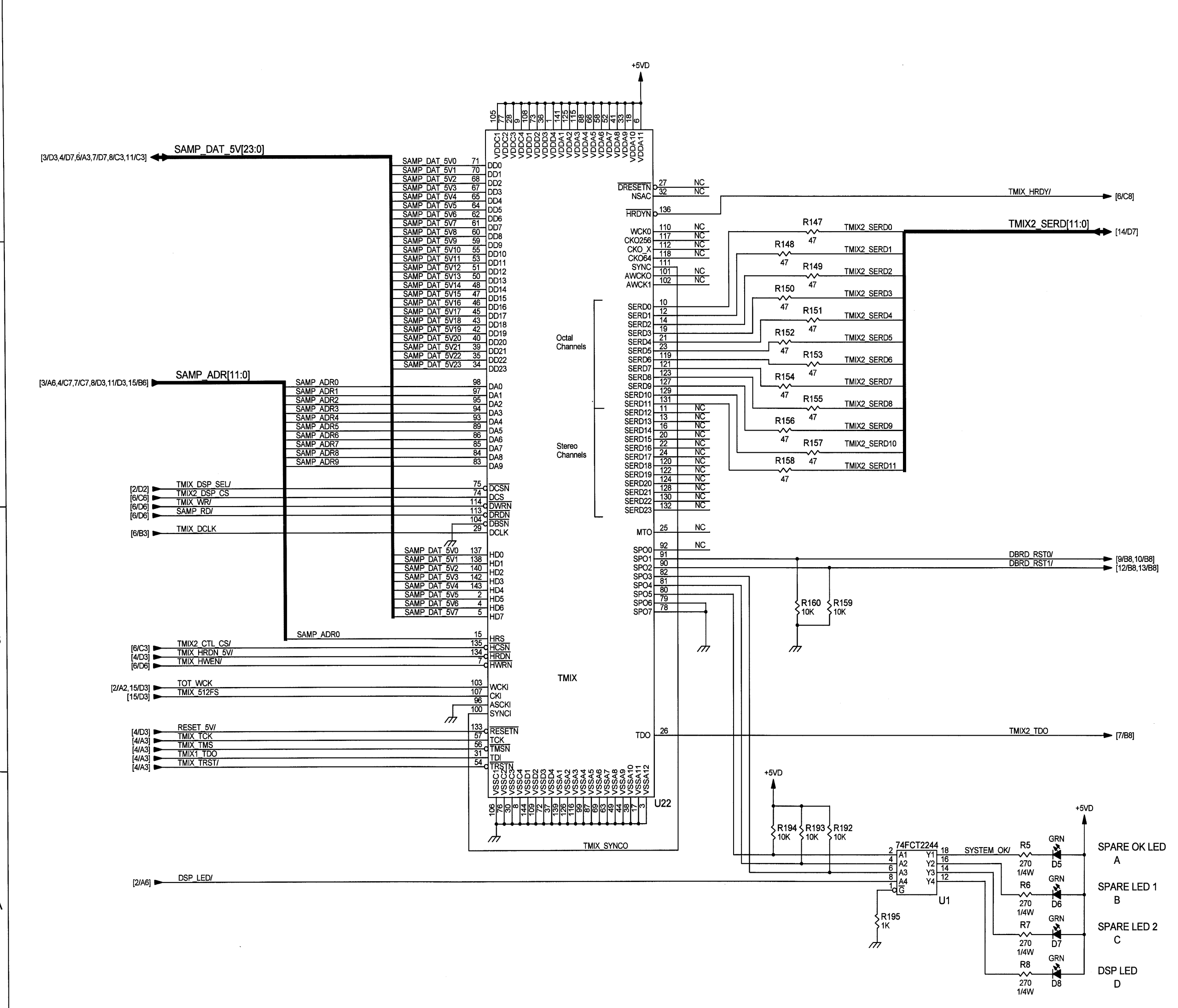
TITLE: SCHEM, RVB BD, 960L LEVEL SHIFTERS

SIZE: B | CODE | NUMBER: 060-13369 | REV: 2

FILE NAME: 13369-2.3 | SHEET 3 OF 16

1-5-2000_15:29


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
TMIX #1
060-13369
SHEET 4 OF 16
1-5-2000 15:30



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991029-01	RWH 10/29/99	CW 11/1/99
		JV 11/1/99	JV 11/2/99
2	CHANGED PER DCR 991208-00	RWH 12/29/99	CW 12/30/99
		JV 12/28/99	PJM 1/5/00

CONTRACT NO.

lexicon

3 OAK PARK
BEDFORD, MA 01730

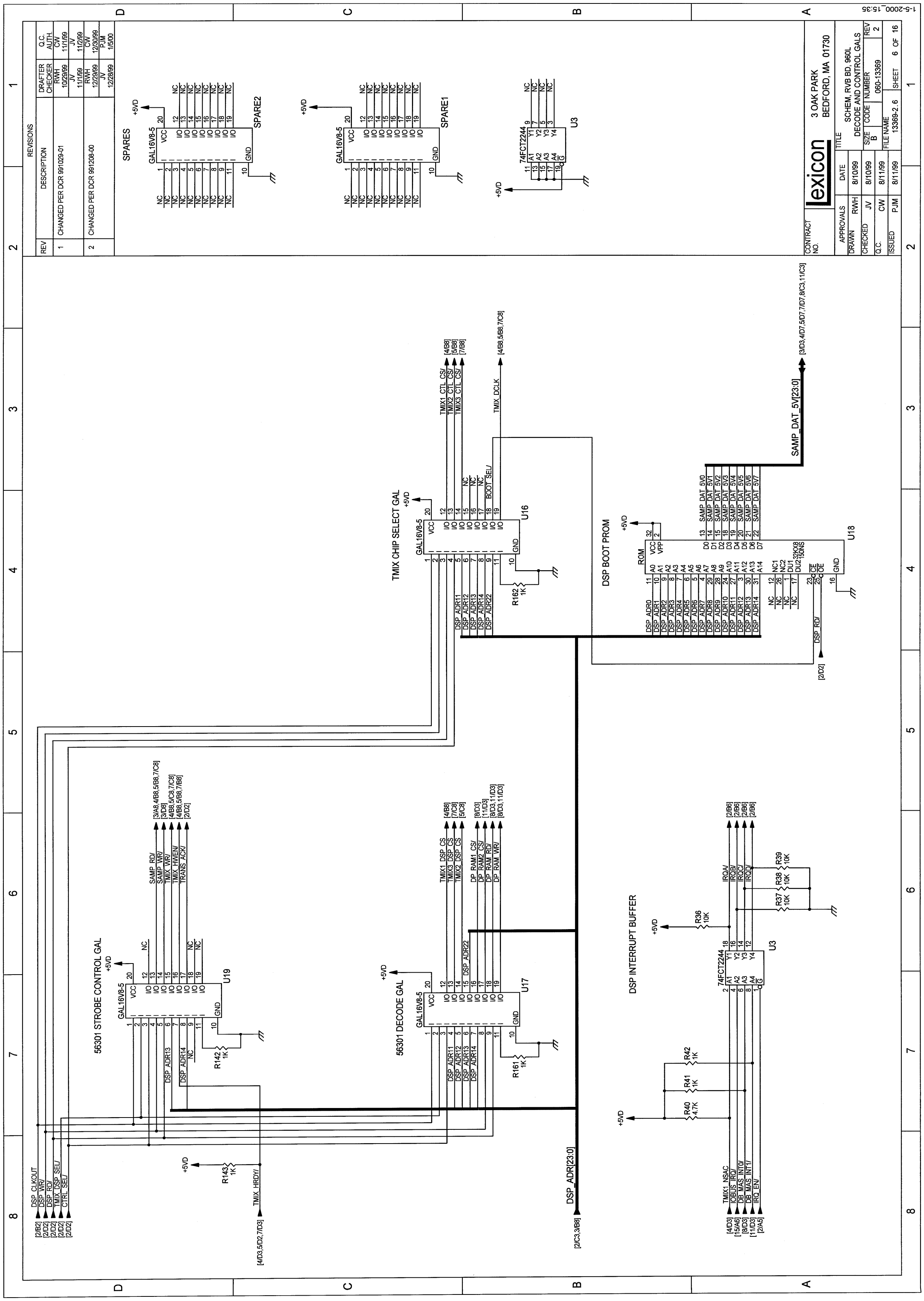
APPROVALS		DATE
DRAWN	RWH	8/10/99
CHECKED	JV	8/10/99
Q.C.	CW	8/11/99
ISSUED	PJM	8/11/99

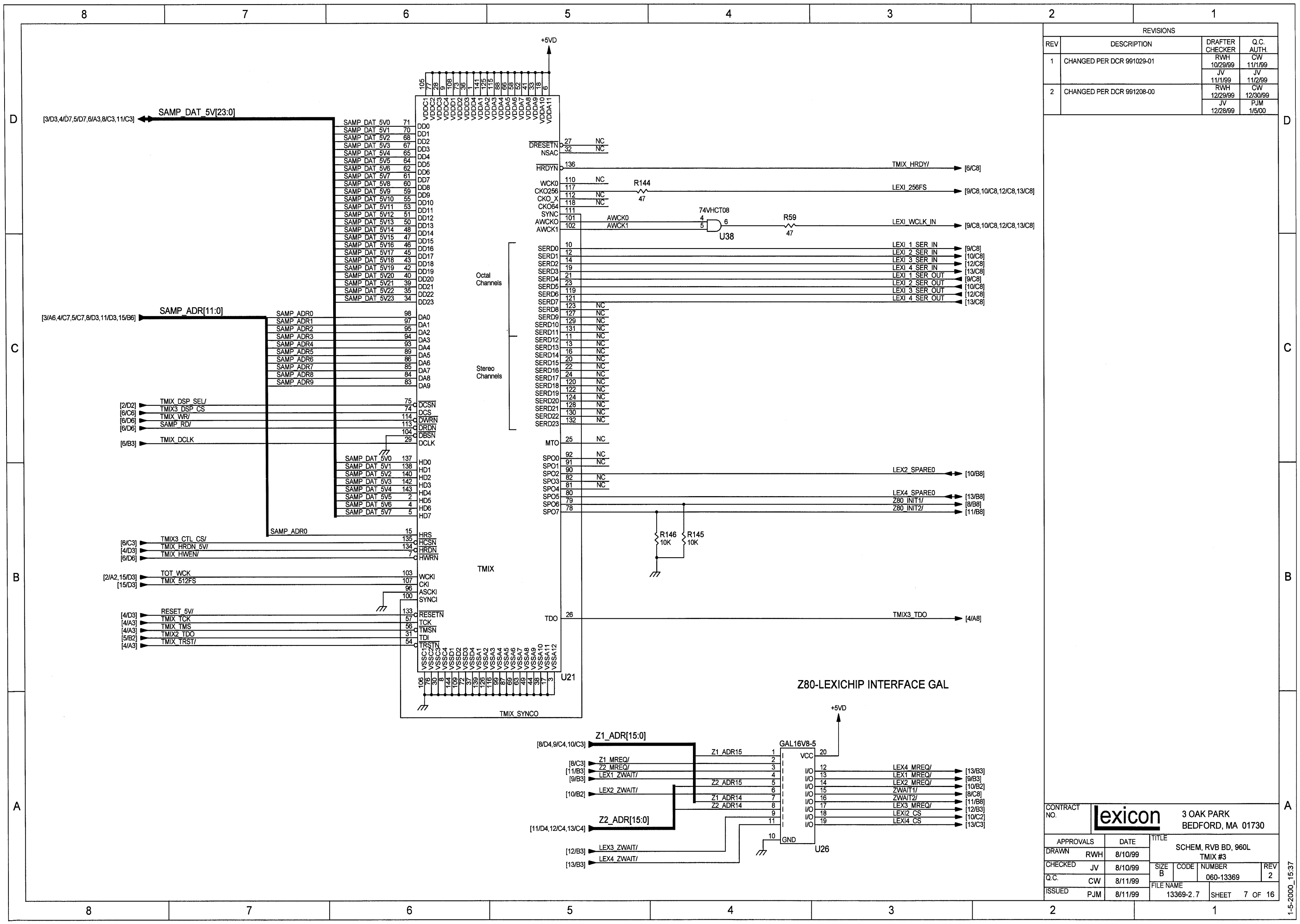
TITLE: SCHEM, RVB BD, 960L
TMIX #2

SIZE: B | CODE | NUMBER: 060-13369 | REV: 2

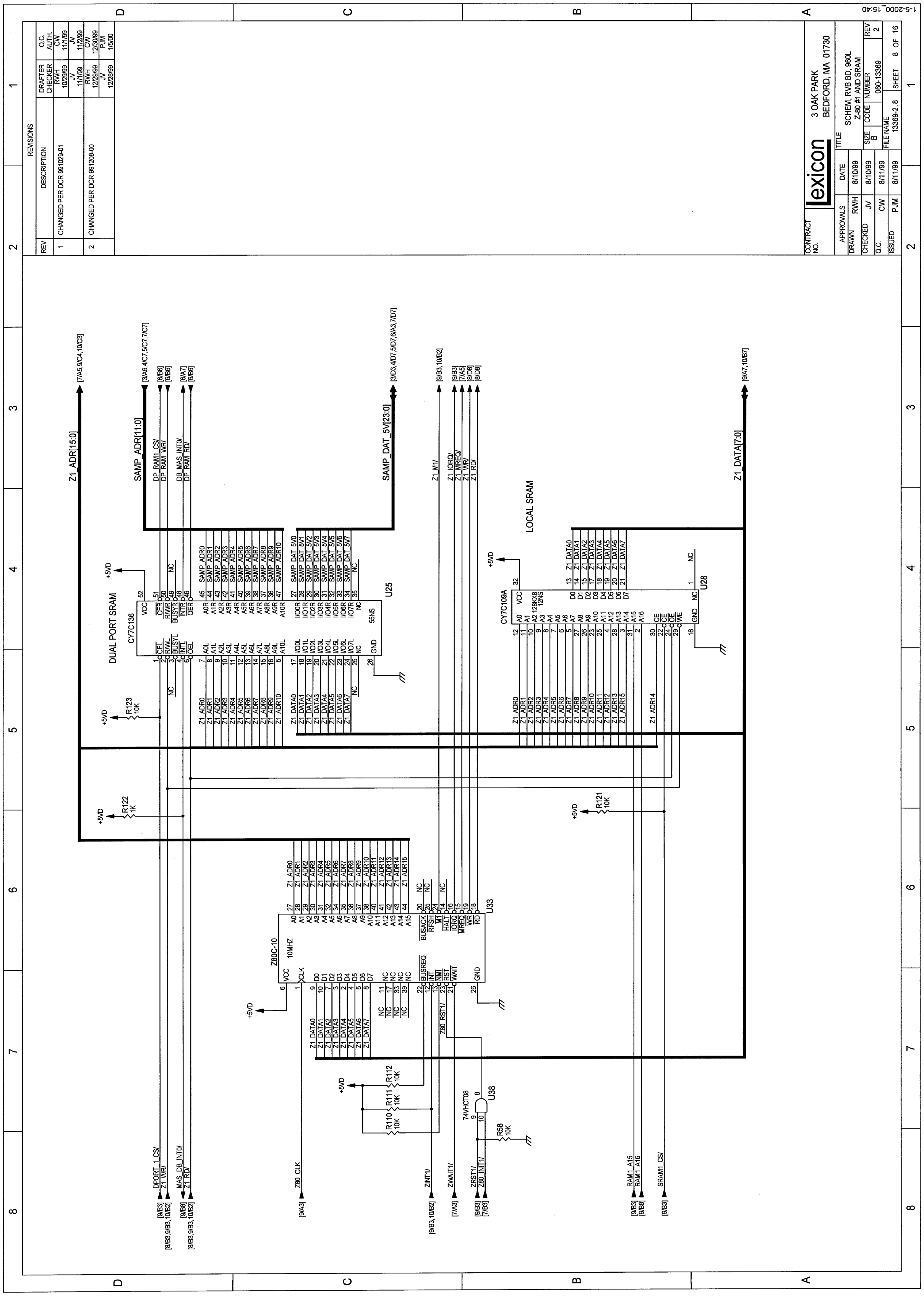
FILE NAME: 13369-2. 5 | SHEET 5 OF 16

1-5-2000_15:34

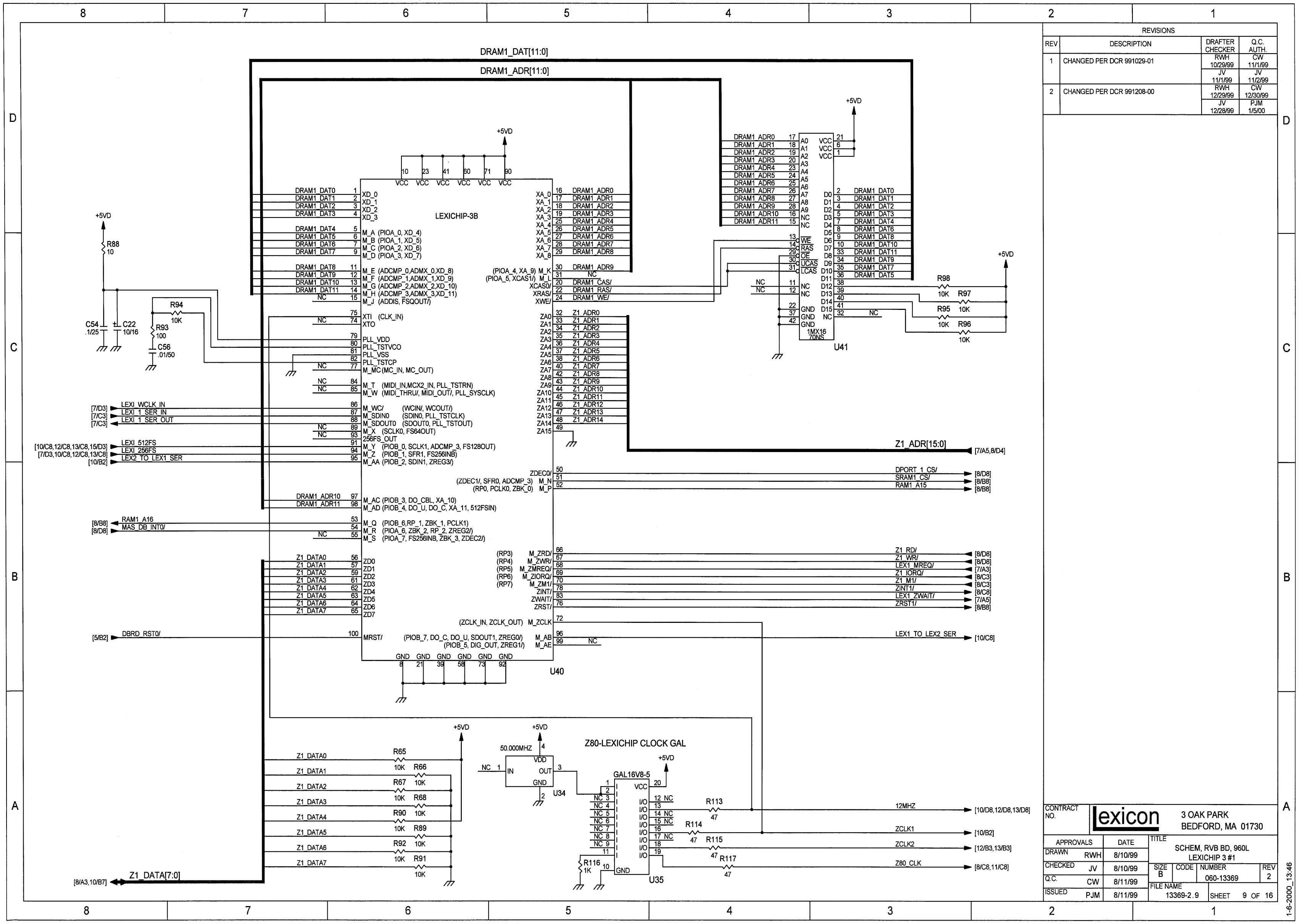

SPARES
SPARE2
SPARE1
TMIX CHIP SELECT GAL
DSP BOOT PROM
56301 STROBE CONTROL GAL
56301 DECODE GAL
DSP INTERRUPT BUFFER
SAMP_DAT_5V[23:0]
DSP_ADR[23:0]
REVISIONS
CHANGED PER DCR 991029-01
CHANGED PER DCR 991208-00
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
DECODE AND CONTROL GALS
060-13369
SHEET 6 OF 16

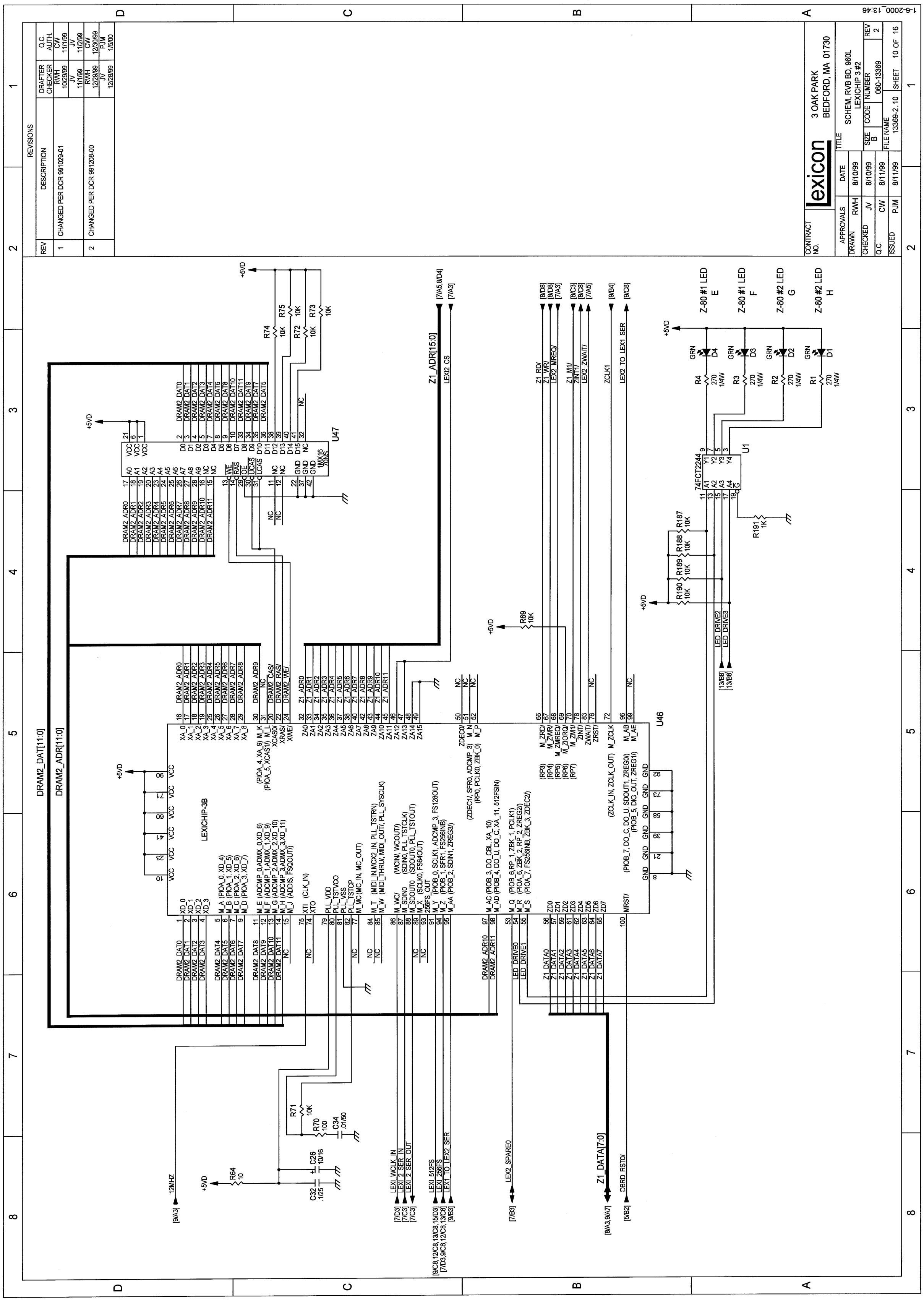


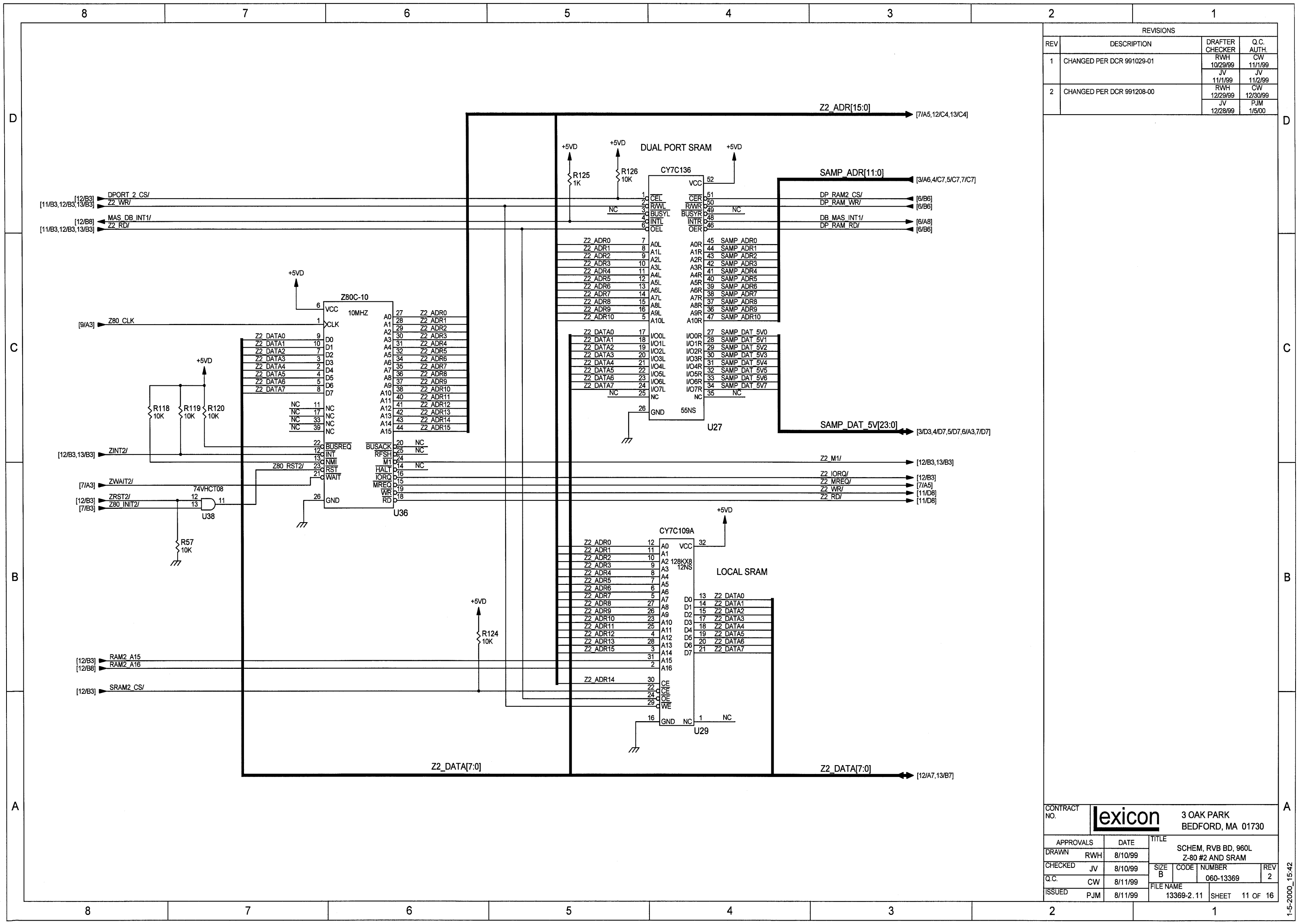
Z80-LEXICHIP INTERFACE GAL
TMIX
U21
U38
74VHCT08
U26
GAL16V8-5
R144
47
R59
47
R146
10K
R145
10K
+5VD
SAMP_DAT_5V[23:0]
SAMP_ADR[11:0]
Z1_ADR[15:0]
Z2_ADR[15:0]
Octal Channels
Stereo Channels
TMIX_SYNCO
TMIX_HRDY/
LEXI_256FS
LEXI_WCLK_IN
LEXI_1_SER_IN
LEXI_2_SER_IN
LEXI_3_SER_IN
LEXI_4_SER_IN
LEXI_1_SER_OUT
LEXI_2_SER_OUT
LEXI_3_SER_OUT
LEXI_4_SER_OUT
LEX2_SPARE0
LEX4_SPARE0
Z80_INIT1/
Z80_INIT2/
TMIX3_TDO
TMIX_DSP_SEL/
TMIX3_DSP_CS
TMIX_WR/
SAMP_RD/
TMIX_DCLK
TMIX3_CTL_CS/
TMIX_HRDN_5V/
TMIX_HWEN/
TOT_WCK
TMIX_512FS
RESET_5V/
TMIX_TCK
TMIX_TMS
TMIX2_TDO
TMIX_TRST/
Z1_MREQ/
Z2_MREQ/
LEX1_ZWAIT/
LEX2_ZWAIT/
LEX3_ZWAIT/
LEX4_ZWAIT/
LEX4_MREQ/
LEX1_MREQ/
LEX2_MREQ/
ZWAIT1/
ZWAIT2/
LEX3_MREQ/
LEXI2_CS
LEXI4_CS
REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991029-01 | RWH 10/29/99 JV 11/1/99 | CW 11/1/99 JV 11/2/99
2 | CHANGED PER DCR 991208-00 | RWH 12/29/99 JV 12/28/99 | CW 12/30/99 PJM 1/5/00
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS | DATE
DRAWN RWH 8/10/99
CHECKED JV 8/10/99
Q.C. CW 8/11/99
ISSUED PJM 8/11/99
TITLE SCHEM, RVB BD, 960L TMIX #3
SIZE B
CODE
NUMBER 060-13369
REV 2
FILE NAME 13369-2.7
SHEET 7 OF 16
1-5-2000_15:37

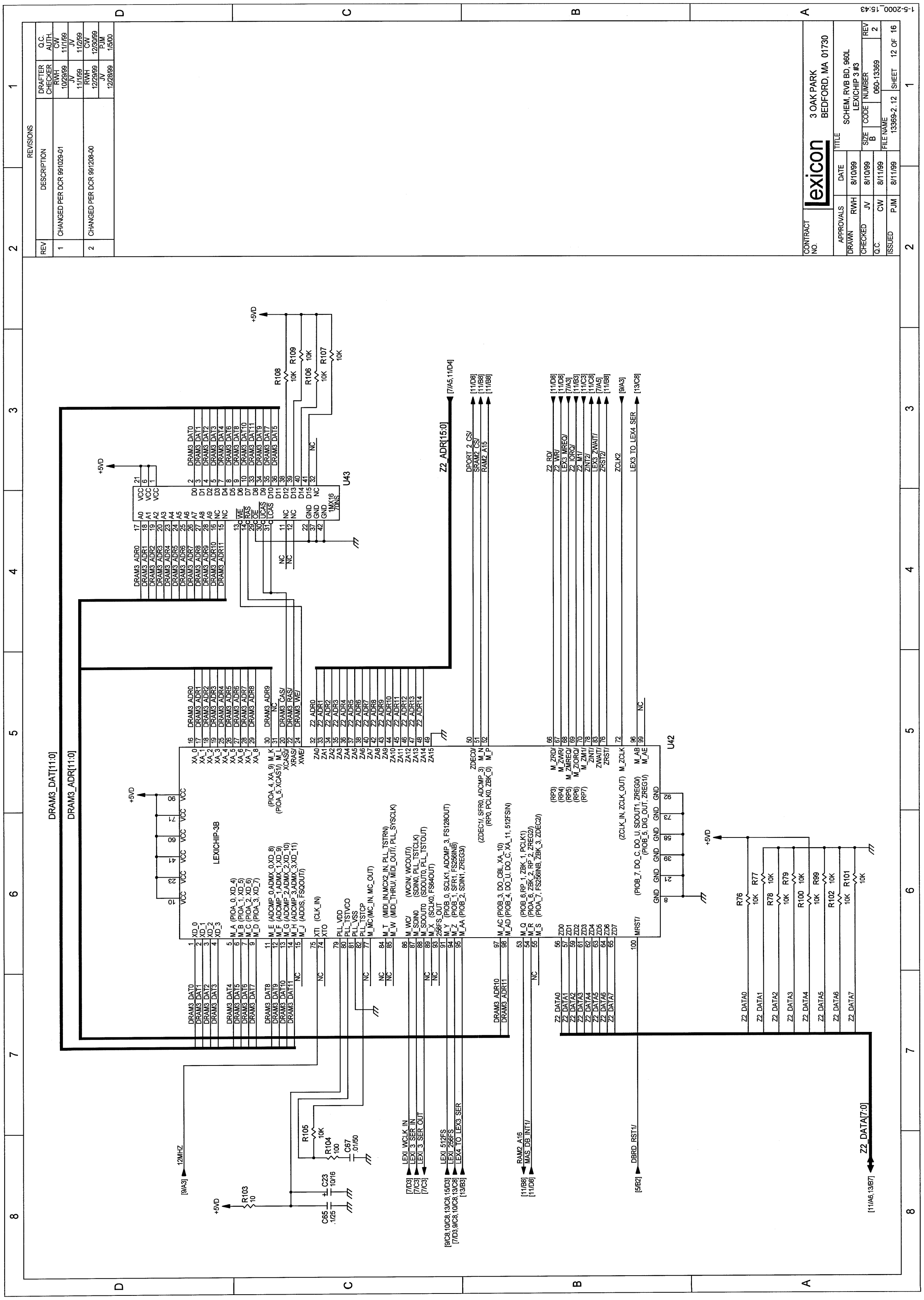


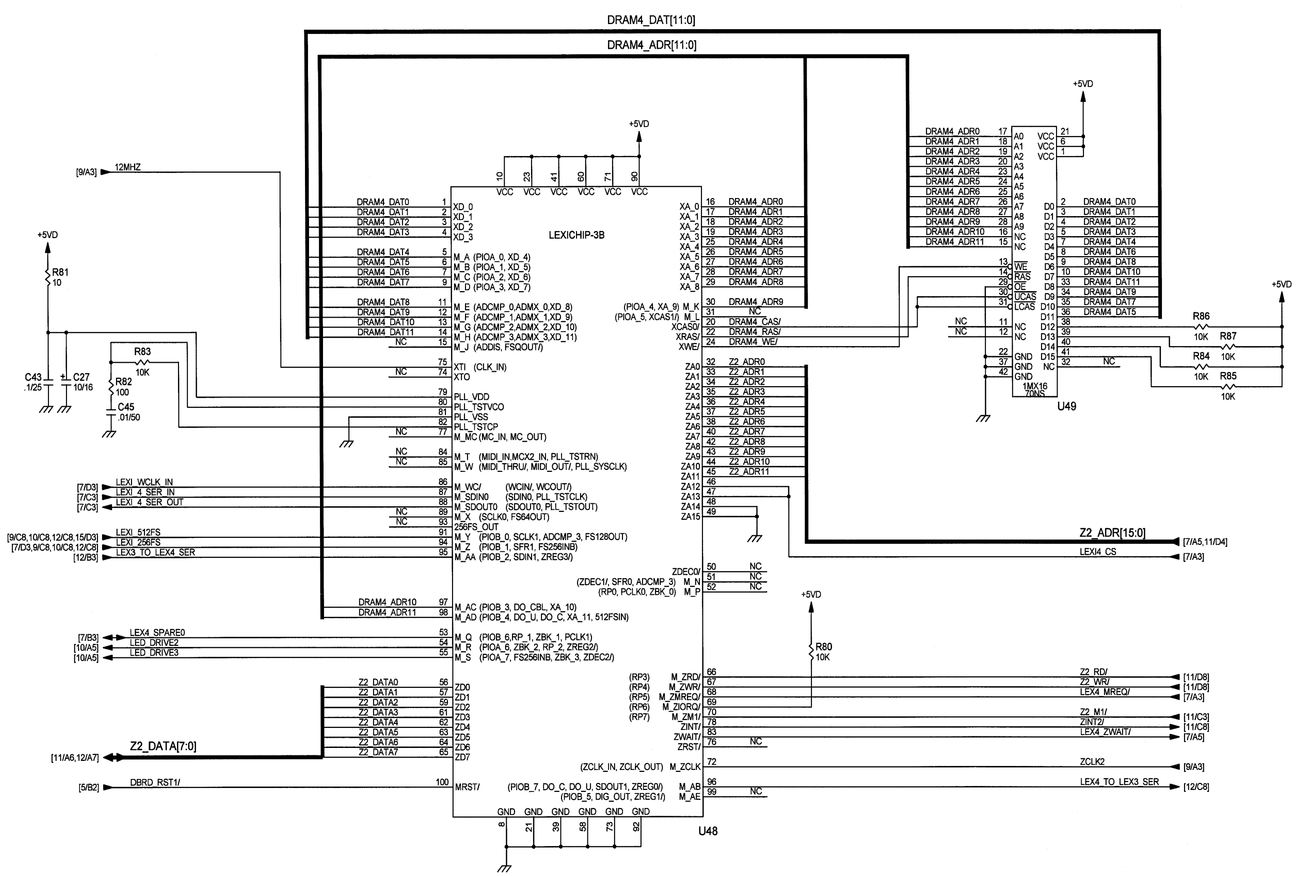
DUAL PORT SRAM
LOCAL SRAM
CY7C136
CY7C109A
Z80C-10
74VHCT08
U25
U28
U33
U38
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
Z-80 #1 AND SRAM
060-13369
13369-2.8
SHEET 8 OF 16


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991029-01 | RWH 10/29/99 JV 11/1/99 | CW 11/1/99 JV 11/2/99
2 | CHANGED PER DCR 991208-00 | RWH 12/29/99 JV 12/28/99 | CW 12/30/99 PJM 1/5/00
DRAM1_DAT[11:0]
DRAM1_ADR[11:0]
LEXICHIP-3B
U40
U41
1MX16 70NS
Z1_ADR[15:0]
Z1_DATA[7:0]
Z80-LEXICHIP CLOCK GAL
GAL16V8-5
U35
U34
50.000MHZ
+5VD
12MHZ
ZCLK1
ZCLK2
Z80_CLK
LEX1_TO_LEX2_SER
DBRD_RST0/
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS | DATE
DRAWN RWH 8/10/99
CHECKED JV 8/10/99
Q.C. CW 8/11/99
ISSUED PJM 8/11/99
TITLE SCHEM, RVB BD, 960L LEXICHIP 3 #1
SIZE B
CODE
NUMBER 060-13369
REV 2
FILE NAME 13369-2. 9
SHEET 9 OF 16
1-6-2000 13:46


3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
LEXICHIP 3 #2
060-13369
10 OF 16


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991029-01 | RWH 10/29/99 JV 11/1/99 | CW 11/1/99 JV 11/2/99
2 | CHANGED PER DCR 991208-00 | RWH 12/29/99 JV 12/28/99 | CW 12/30/99 PJM 1/5/00
Z2_ADR[15:0]
DUAL PORT SRAM
CY7C136
U27
SAMP_ADR[11:0]
SAMP_DAT_5V[23:0]
Z80C-10
10MHZ
U36
74VHCT08
U38
CY7C109A
128KX8 12NS
LOCAL SRAM
U29
Z2_DATA[7:0]
DPORT_2_CS/
Z2_WR/
MAS_DB_INT1/
Z2_RD/
Z80_CLK
ZINT2/
ZWAIT2/
ZRST2/
Z80_INIT2/
RAM2_A15
RAM2_A16
SRAM2_CS/
DP_RAM2_CS/
DP_RAM_WR/
DB_MAS_INT1/
DP_RAM_RD/
Z2_M1/
Z2_IORQ/
Z2_MREQ/
Z2_WR/
Z2_RD/
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS | DATE
DRAWN RWH 8/10/99
CHECKED JV 8/10/99
Q.C. CW 8/11/99
ISSUED PJM 8/11/99
TITLE SCHEM, RVB BD, 960L Z-80 #2 AND SRAM
SIZE B
NUMBER 060-13369
REV 2
FILE NAME 13369-2.11
SHEET 11 OF 16
1-5-2000_15:42


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
LEXICHIP 3 #3
060-13369
13369-2.12
SHEET 12 OF 16
U42
U43
LEXICHIP-3B
Z2_DATA[7:0]
Z2_ADR[15:0]
DRAM3_DAT[11:0]
DRAM3_ADR[11:0]



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991029-01	RWH 10/29/99 JV 11/1/99	CW 11/1/99 JV 11/2/99
2	CHANGED PER DCR 991208-00	RWH 12/29/99 JV 12/28/99	CW 12/30/99 PJM 1/5/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

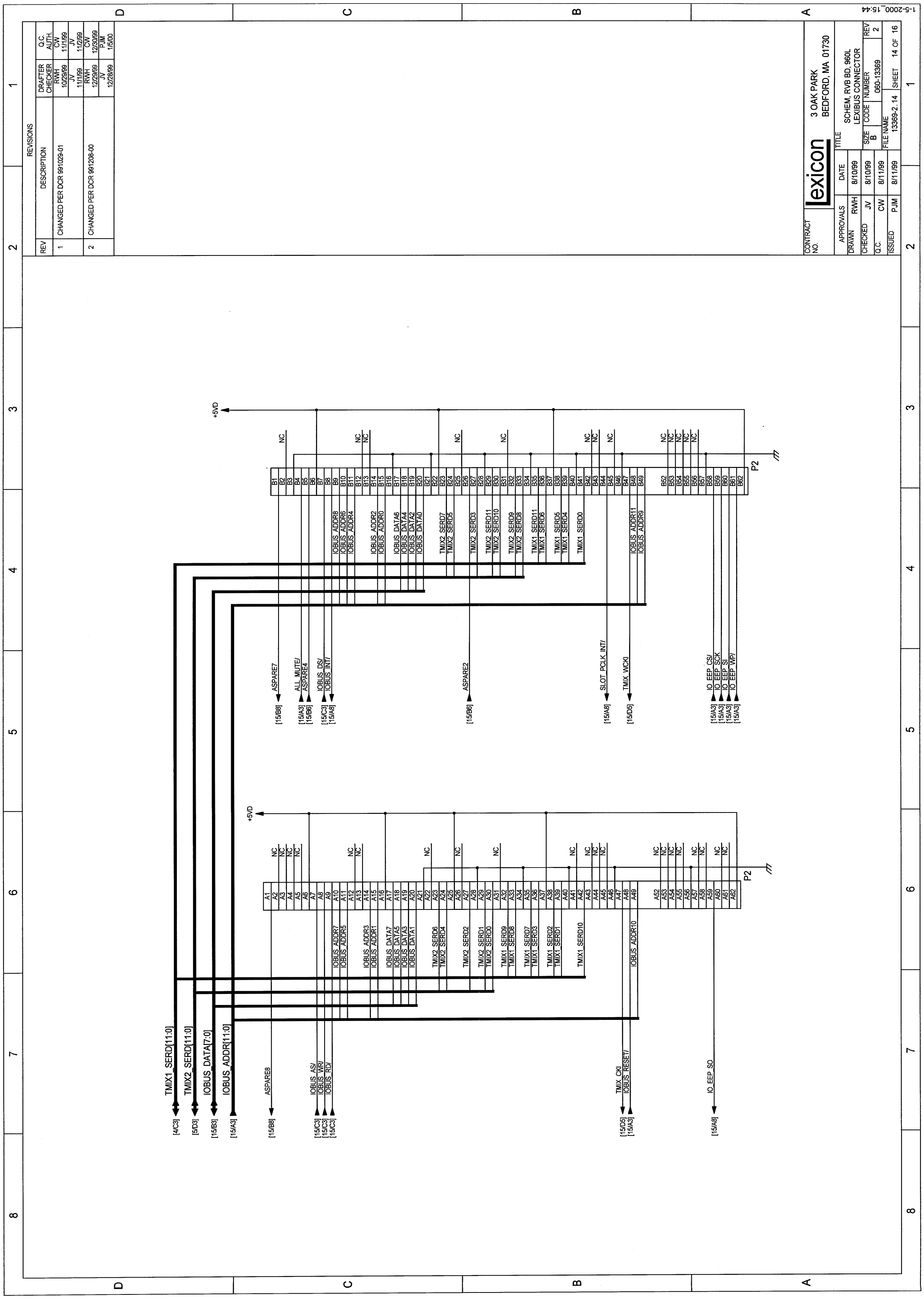
APPROVALS		DATE
DRAWN	RWH	8/10/99
CHECKED	JV	8/10/99
Q.C.	CW	8/11/99
ISSUED	PJM	8/11/99

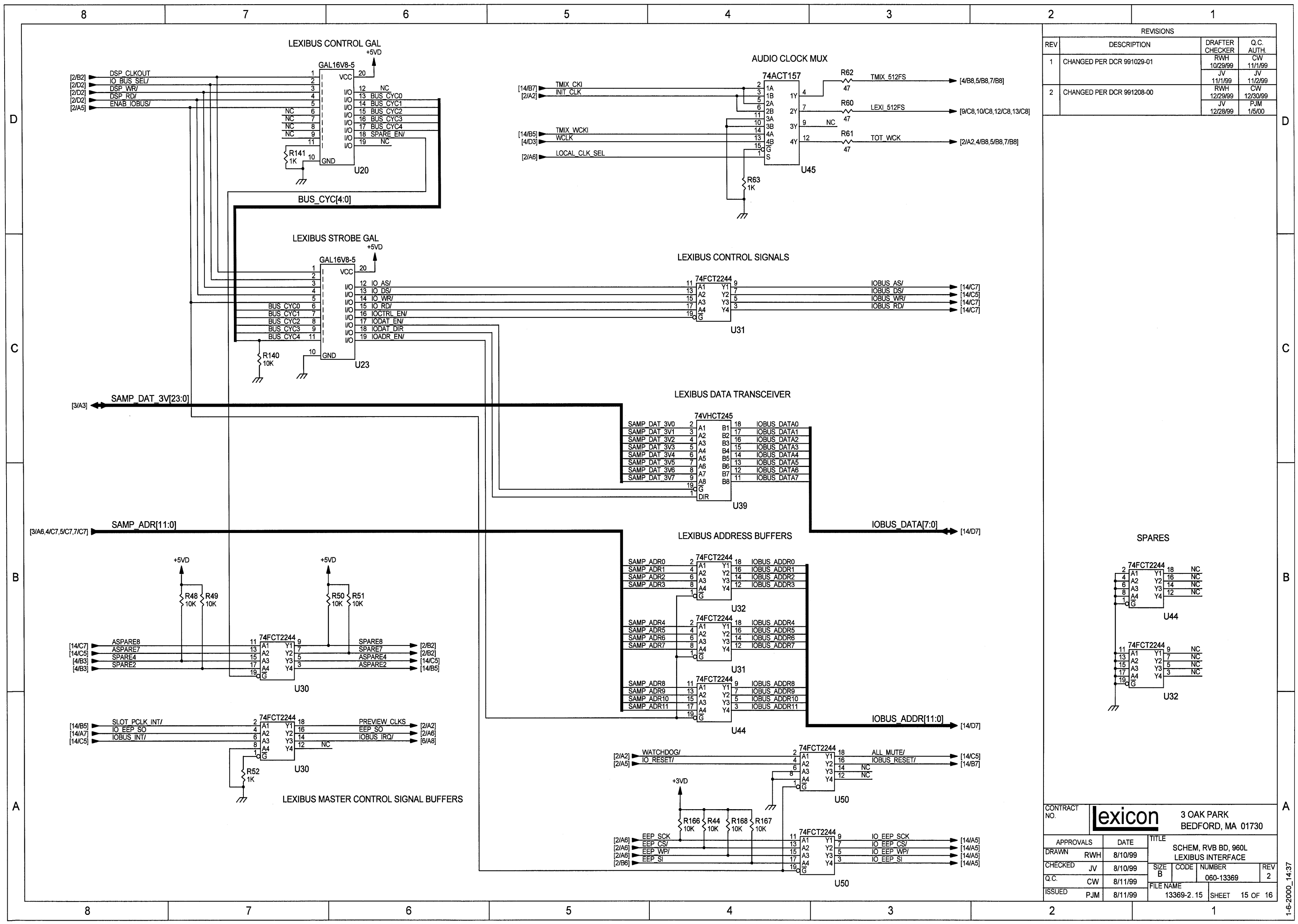
TITLE SCHEM, RVB BD, 960L LEXICHIP 3 #4

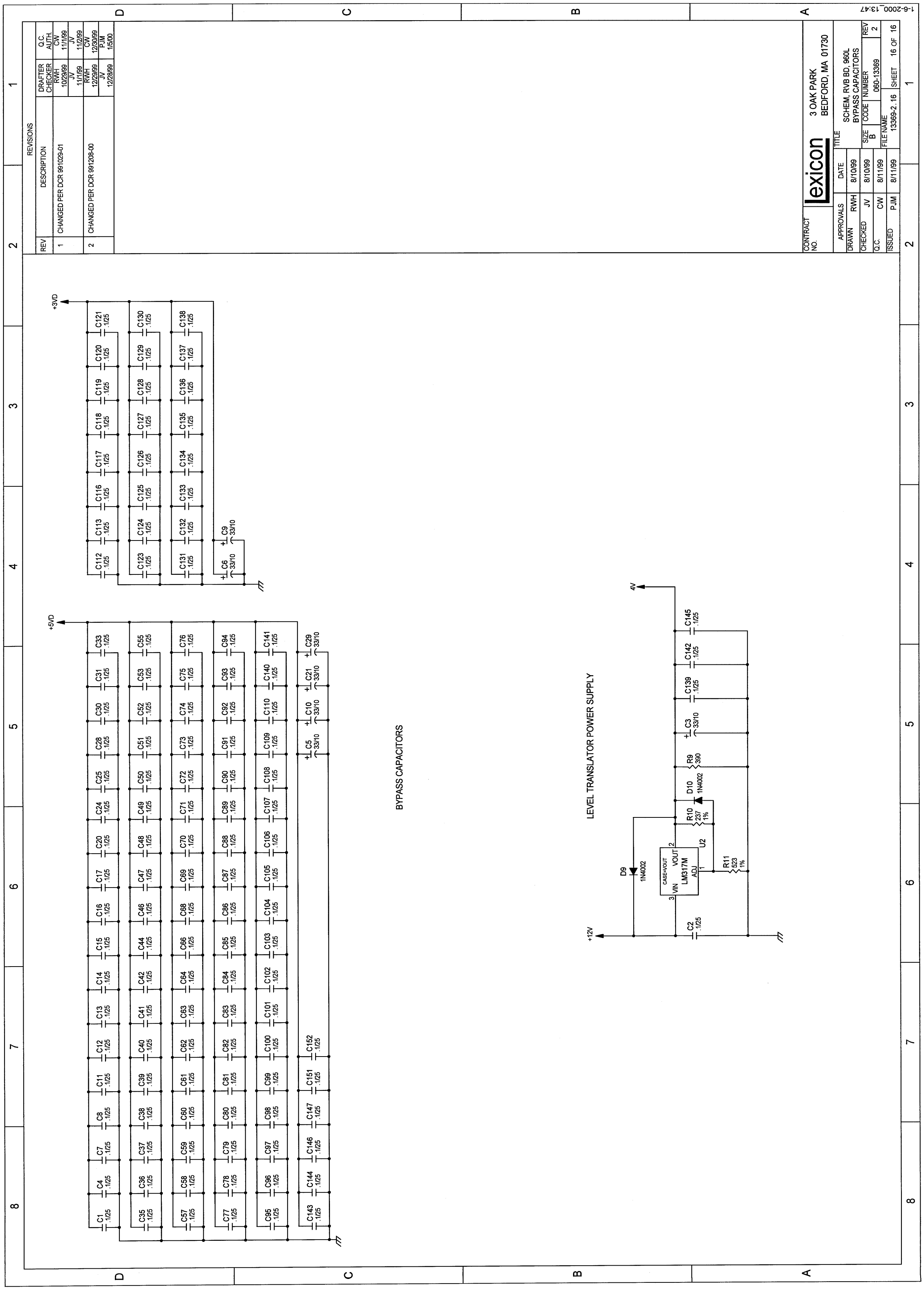
SIZE B | CODE | NUMBER 060-13369 | REV 2

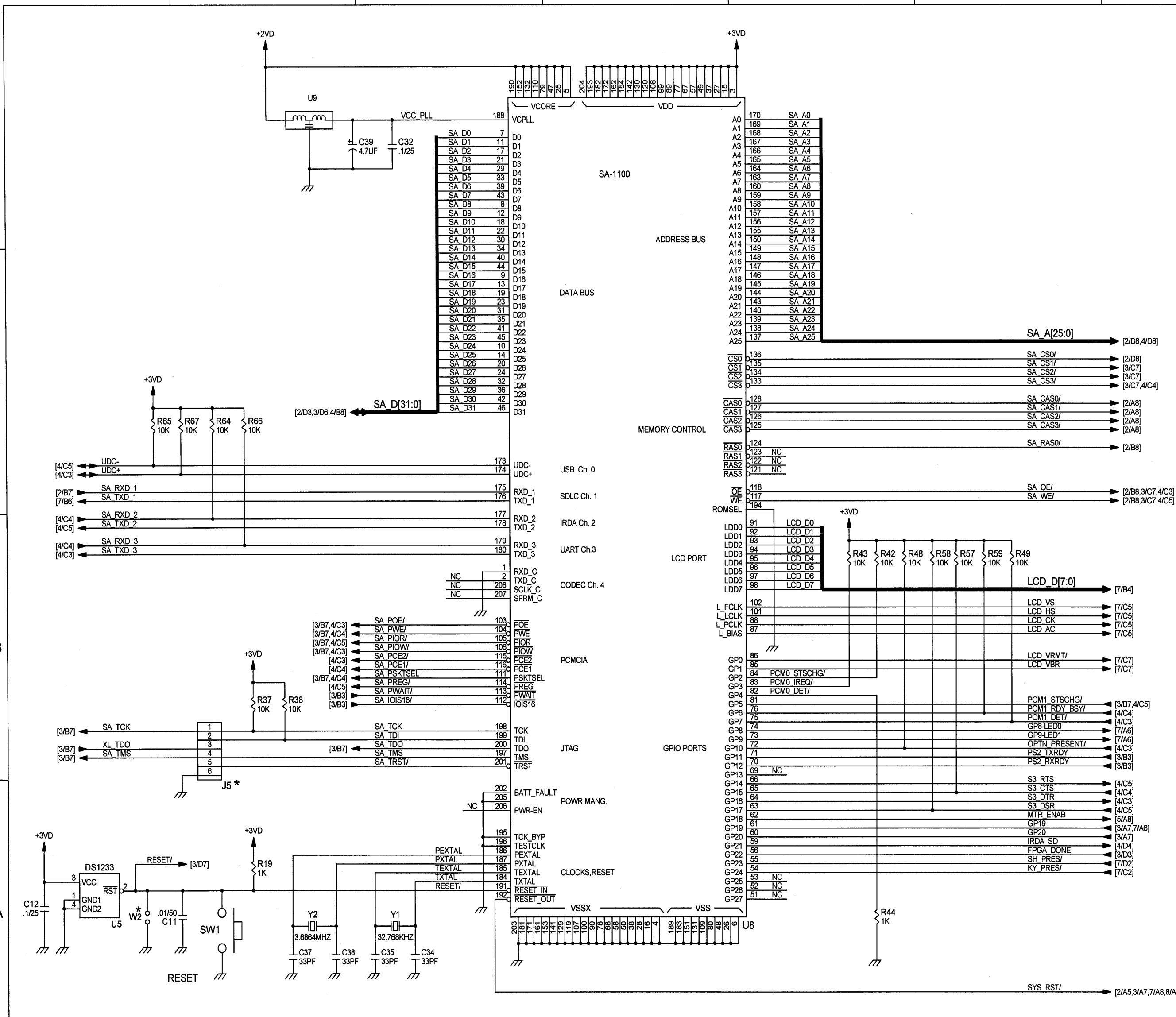
FILE NAME 13369-2. 13 | SHEET 13 OF 16

1-5-2000_15:43


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
LEXIBUS CONNECTOR
060-13369
13369-2.14
SHEET 14 OF 16
CHANGED PER DCR 991029-01
CHANGED PER DCR 991208-00
TMIX1_SERD[11:0]
TMIX2_SERD[11:0]
IOBUS_DATA[7:0]
IOBUS_ADDR[11:0]
P2
+5VD


LEXIBUS CONTROL GAL
GAL16V8-5
U20
AUDIO CLOCK MUX
74ACT157
U45
TMIX_512FS
LEXI_512FS
TOT_WCK
BUS_CYC[4:0]
LEXIBUS STROBE GAL
GAL16V8-5
U23
LEXIBUS CONTROL SIGNALS
74FCT2244
U31
IOBUS_AS/
IOBUS_DS/
IOBUS_WR/
IOBUS_RD/
SAMP_DAT_3V[23:0]
LEXIBUS DATA TRANSCEIVER
74VHCT245
U39
IOBUS_DATA[7:0]
SAMP_ADR[11:0]
LEXIBUS ADDRESS BUFFERS
U32
U31
U44
IOBUS_ADDR[11:0]
SPARES
U44
U32
U30
LEXIBUS MASTER CONTROL SIGNAL BUFFERS
U50
REVISIONS
REV
DESCRIPTION
DRAFTER CHECKER
Q.C. AUTH.
1
CHANGED PER DCR 991029-01
RWH 10/29/99
CW 11/1/99
JV 11/1/99
JV 11/2/99
2
CHANGED PER DCR 991208-00
RWH 12/29/99
CW 12/30/99
JV 12/28/99
PJM 1/5/00
CONTRACT NO.
lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS
DATE
DRAWN RWH 8/10/99
CHECKED JV 8/10/99
Q.C. CW 8/11/99
ISSUED PJM 8/11/99
TITLE
SCHEM, RVB BD, 960L
LEXIBUS INTERFACE
SIZE B
CODE
NUMBER 060-13369
REV 2
FILE NAME 13369-2.15
SHEET 15 OF 16
1-6-2000_14:37


BYPASS CAPACITORS
LEVEL TRANSLATOR POWER SUPPLY
LM317M
3 OAK PARK
BEDFORD, MA 01730
SCHEM, RVB BD, 960L
BYPASS CAPACITORS
060-13369
SHEET 16 OF 16



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991015-00	RWH 10/15/99 GHL 11/11/99	CW 11/12/99 PJM 11/12/99
2	CHANGED PER DCR 991221-01	RWH 12/27/99 ECM 1/4/00	CW 1/5/00 PJM 1/5/00
3	RENAMED PWR_OK TO RESET/, CHANGED SHEETS 3, 7 PER ECO 000217-00 & A	RWH 3/10/00 ECM 3/10/00	CW 3/10/00 PJM 3/10/00
4	CHANGED SHEET 3 PER ECO 000802-00	RWH 8/2/00 ECM 8/2/00	CW 8/2/00 JV 8/2/00

NOTES

1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W

2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%

3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V

4 DIGITAL GROUND; ANALOG GROUND; CHASSIS GROUND; POWER GROUND

5 [XX/XX] DENOTES [SHEET NUMBER/SECTOR]

6 COMPONENTS MARKED WITH * ARE NOT INSTALLED

7 LAST REFERENCE DESIGNATORS USED: C153, D39, FB10, J21, L1, PS1, Q9, R146, SW1, U41, W2, Y2.

DOCUMENT CONTROL BLOCK: #060-13379

SHEET NUMBER	REVISION NUMBER
1 OF 9	4
2 OF 9	2
3 OF 9	4
4 OF 9	2
5 OF 9	2
6 OF 9	2
7 OF 9	3
8 OF 9	2
9 OF 9	2

CONTRACT NO.

lexicon — 3 OAK PARK, BEDFORD, MA 01730

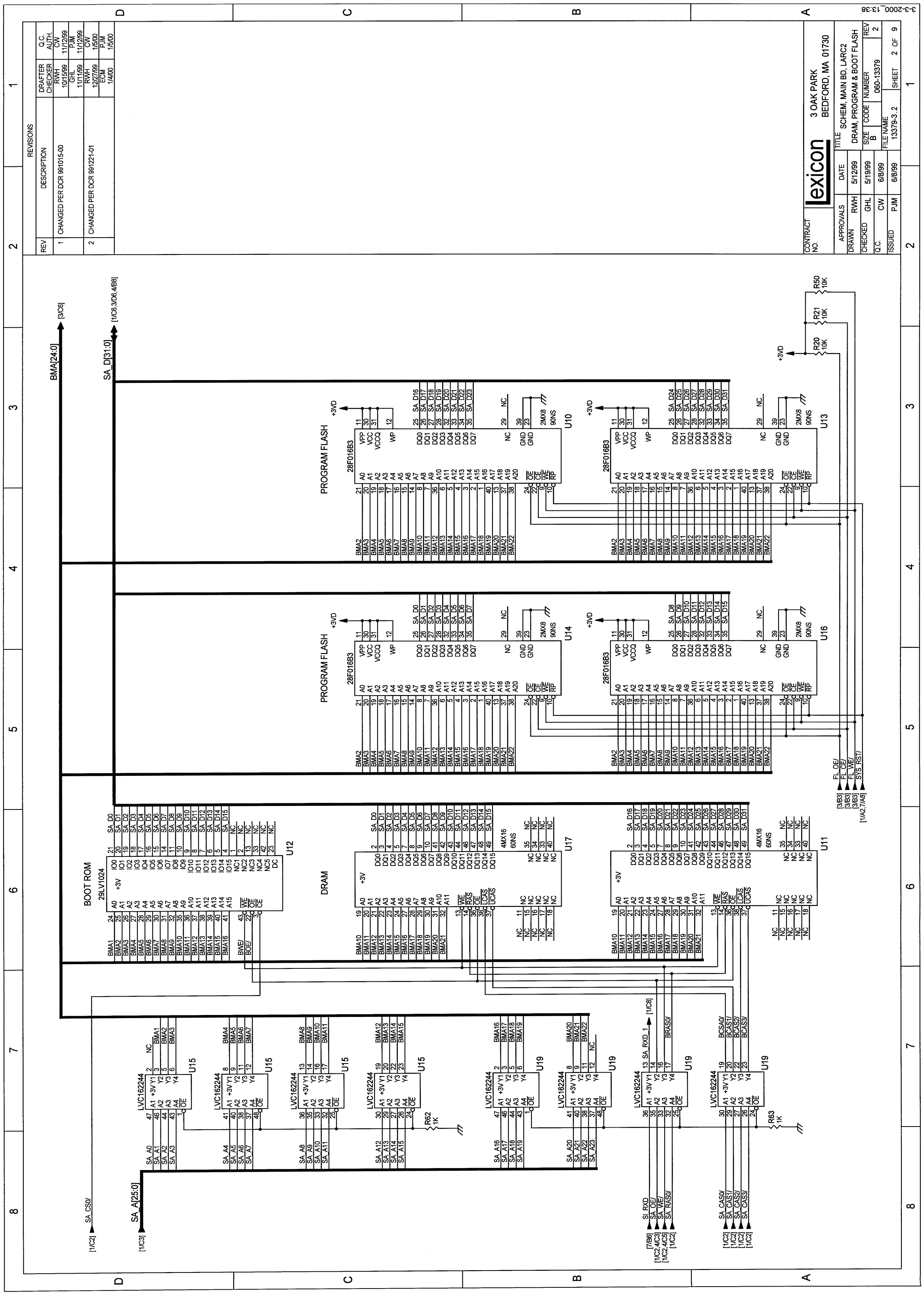
APPROVALS		DATE
DRAWN	RWH	5/12/99
CHECKED	GHL	5/19/99
Q.C.	CW	6/8/99
ISSUED	PJM	6/8/99

TITLE: SCHEM, MAIN BD, LARC2 SA-1100 CPU

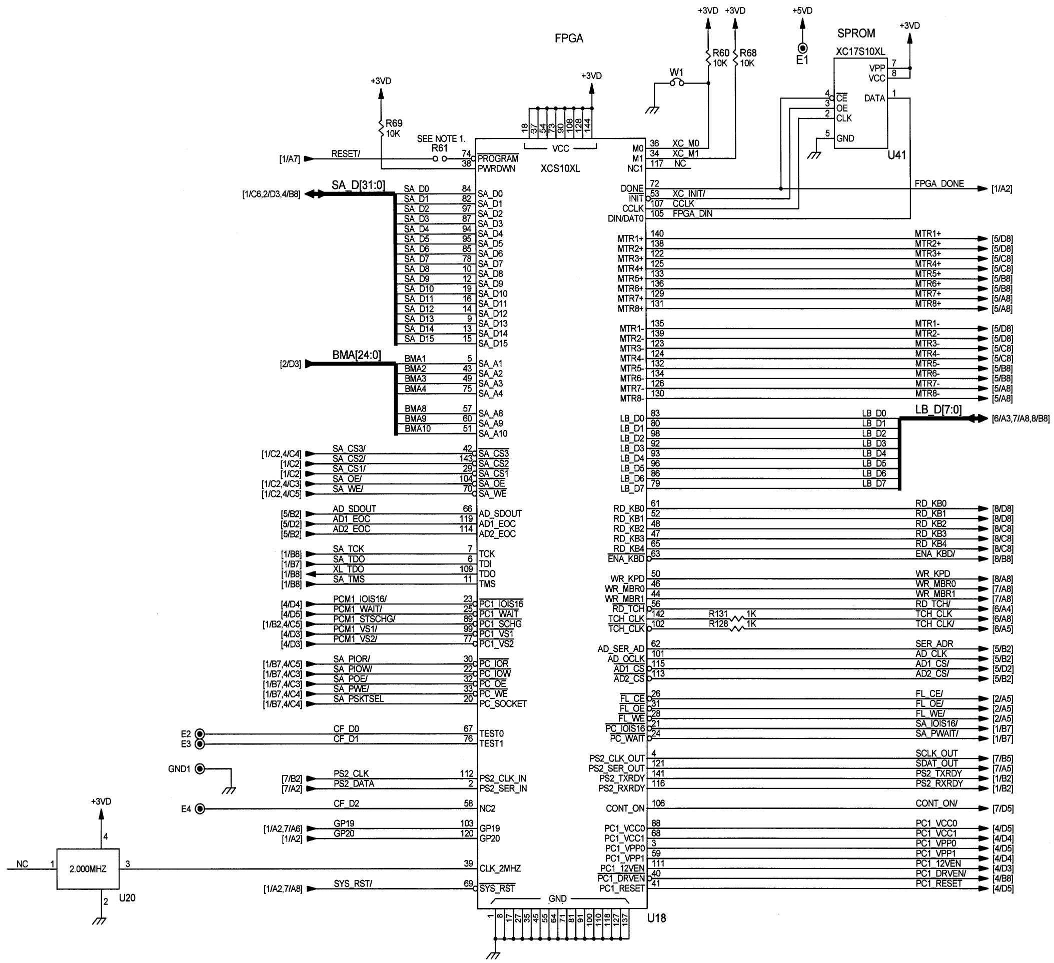
SIZE: B | CODE | NUMBER: 060-13379 | REV: 4

FILE NAME: 13379-4.1 | SHEET 1 OF 9

8-2-2000_17:10



PROGRAM FLASH
BOOT ROM
DRAM
3 OAK PARK
BEDFORD, MA 01730
SCHEM, MAIN BD, LARC2
DRAM, PROGRAM & BOOT FLASH
060-13379
SHEET 2 OF 9



REVISIONS			
REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991015-00	RWH 10/15/99 GHL 11/11/99	CW 11/12/99 PJM 11/12/99
2	CHANGED PER DCR 991221-01	RWH 12/27/99 ECM 1/4/00	CW 1/5/00 PJM 1/5/00
3	TIE RESET/ TO U18.74 PER ECO 000217-00 & A	RWH 3/10/00 ECM 3/10/00	CW 3/10/00 PJM 3/10/00
4	DISCONNECT RESET/ FROM U18.74 USING JUMPER R61 PER ECO 000802-00	RWH 8/2/00 ECM 8/2/00	CW 8/2/00 JV 8/2/00

NOTES

1 R61 IS TO BE POPULATED ONLY IF CALLED OUT ON BOM.

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

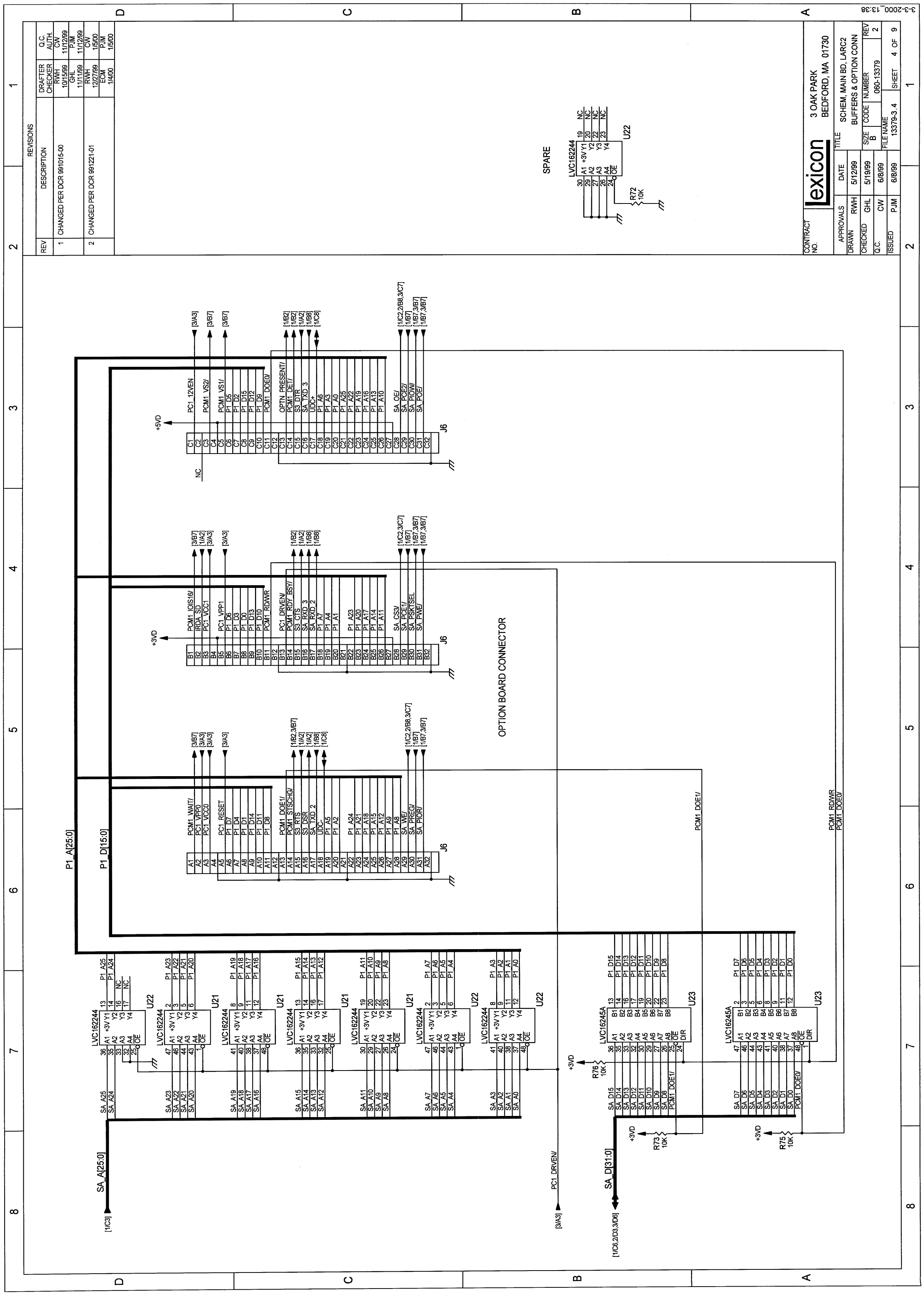
APPROVALS		DATE
DRAWN	RWH	5/12/99
CHECKED	GHL	5/19/99
Q.C.	CW	6/8/99
ISSUED	PJM	6/8/99

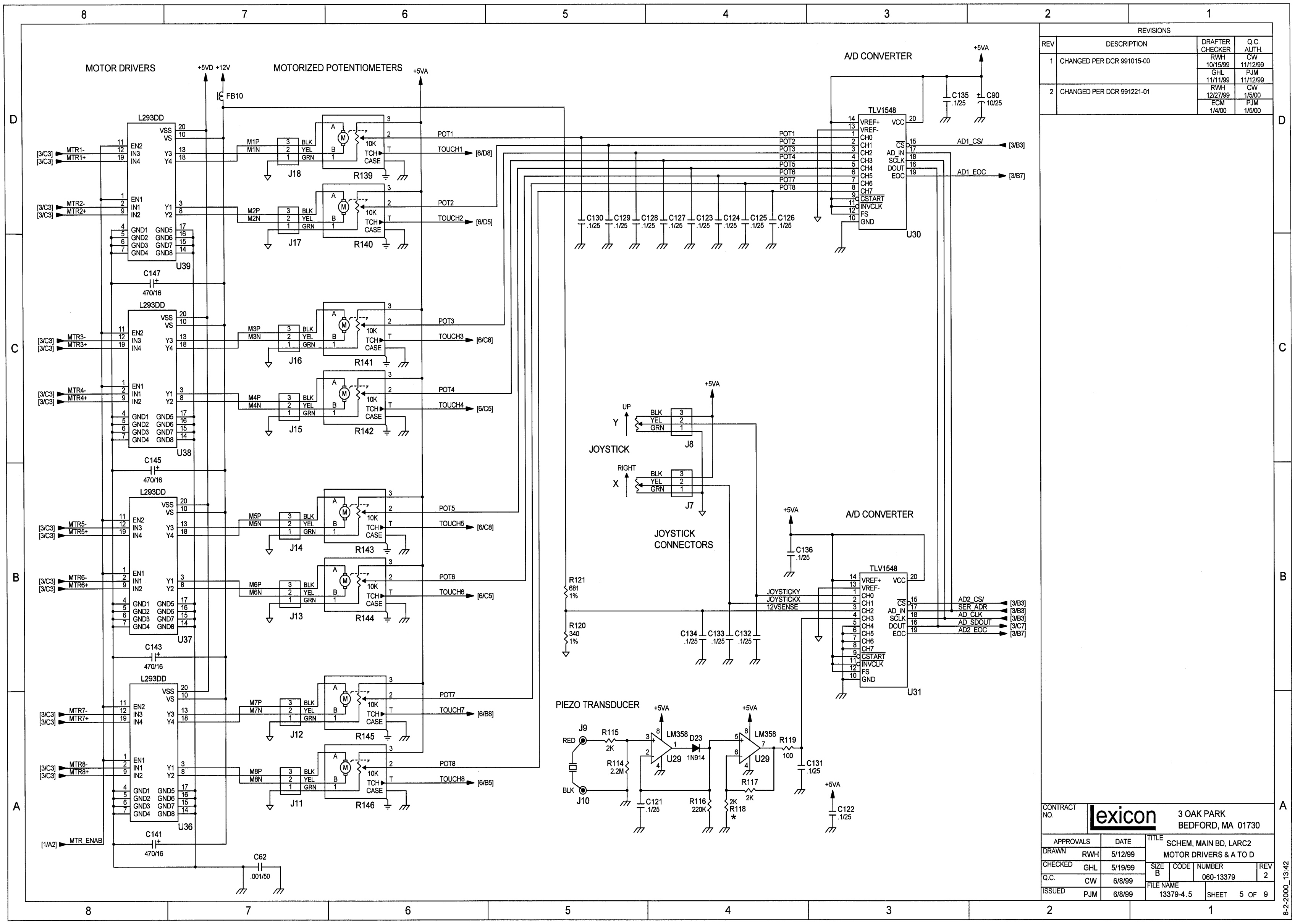
TITLE SCHEM, MAIN BD, LARC2 LARC2 CONTROL

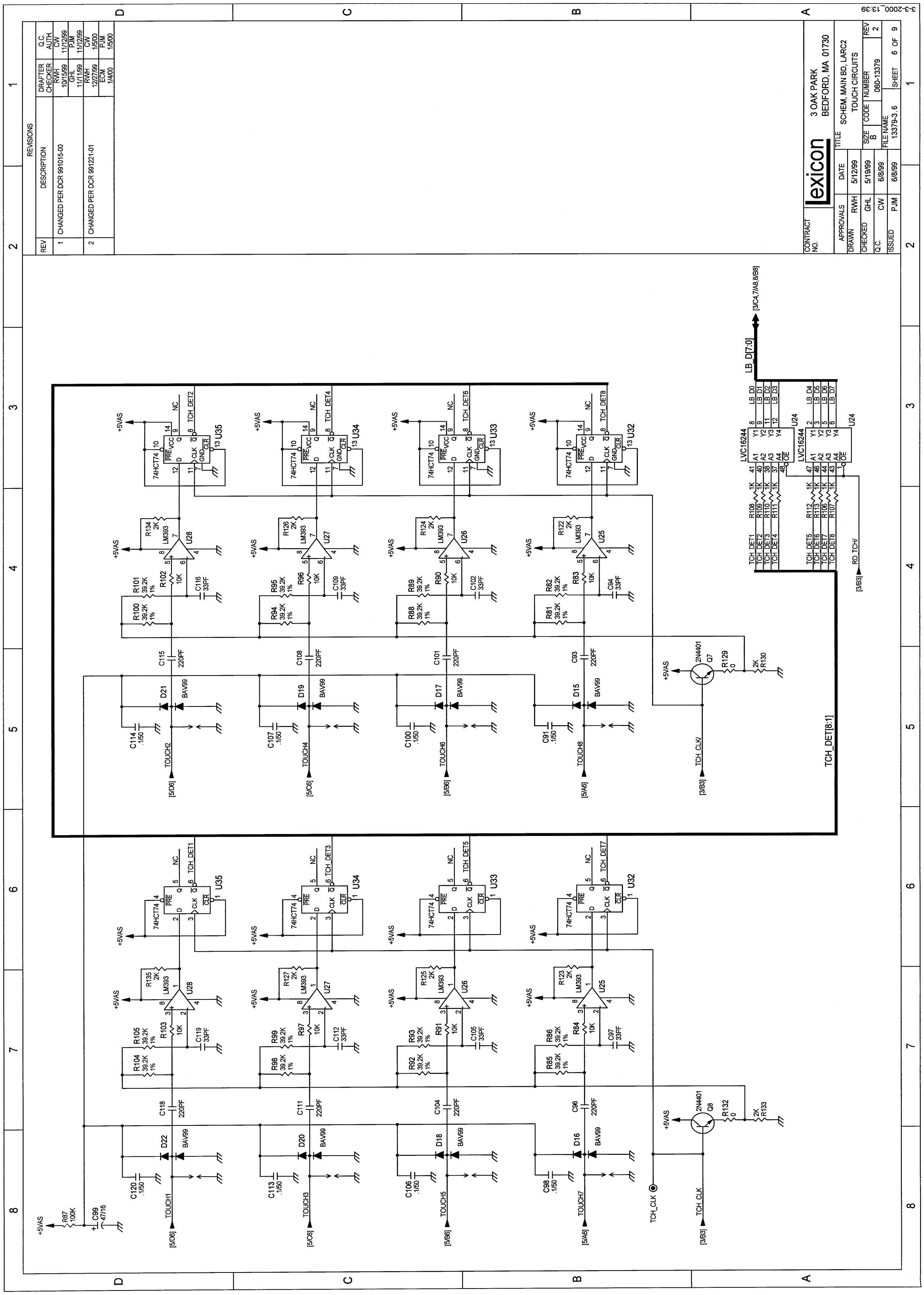
SIZE B | CODE | NUMBER 060-13379 | REV 4

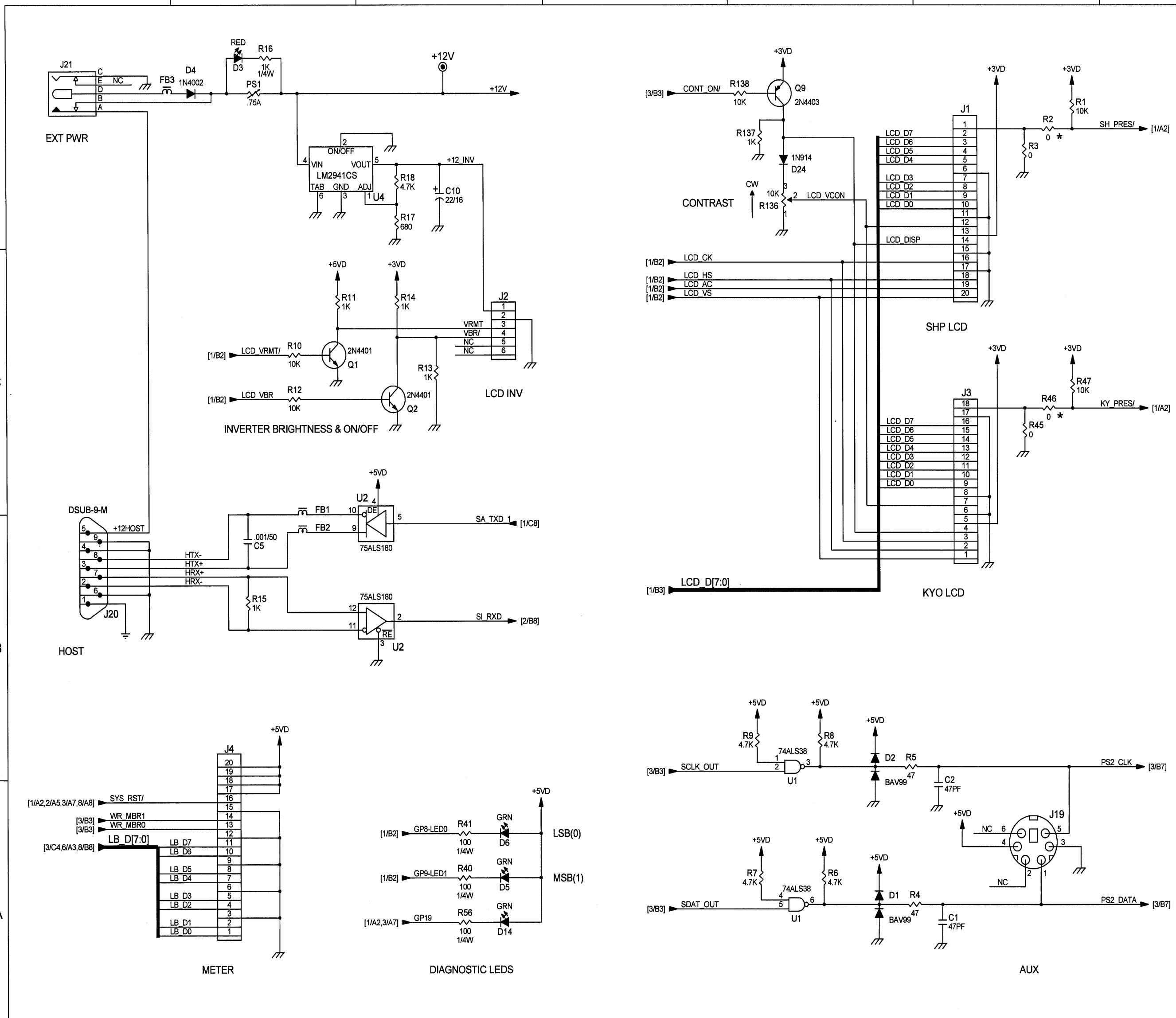
FILE NAME 13379-4.3 | SHEET 3 OF 9

8-2-2000 17:19


OPTION BOARD CONNECTOR
SPARE
REVISIONS
1 CHANGED PER DCR 991015-00
2 CHANGED PER DCR 991221-01
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, MAIN BD, LARC2
BUFFERS & OPTION CONN
060-13379
13379-3_4
SHEET 4 OF 9
3-3-2000 13:38


MOTOR DRIVERS
MOTORIZED POTENTIOMETERS
A/D CONVERTER
JOYSTICK
JOYSTICK CONNECTORS
PIEZO TRANSDUCER
REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991015-00 | RWH 10/15/99 GHL 11/11/99 | CW 11/12/99 PJM 11/12/99
2 | CHANGED PER DCR 991221-01 | RWH 12/27/99 ECM 1/4/00 | CW 1/5/00 PJM 1/5/00
CONTRACT NO.
Lexicon
3 OAK PARK
BEDFORD, MA 01730
APPROVALS | DATE
DRAWN RWH 5/12/99
CHECKED GHL 5/19/99
Q.C. CW 6/8/99
ISSUED PJM 6/8/99
TITLE SCHEM, MAIN BD, LARC2
MOTOR DRIVERS & A TO D
SIZE B
CODE
NUMBER 060-13379
REV 2
FILE NAME 13379-4.5
SHEET 5 OF 9
8-2-2000 13:42


REVISIONS
1 CHANGED PER DCR 991015-00
2 CHANGED PER DCR 991221-01
lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, MAIN BD, LARC2
TOUCH CIRCUITS
060-13379
13379-3_6
SHEET 6 OF 9
LB_D[7:0]
TCH_DET[8:1]
TCH_CLK
TCH_CLK/
RD_TCH/
LVC16244
74HCT74
LM393
BAV99
2N4401



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991015-00	RWH 10/15/99 GHL 11/11/99	CW 11/12/99 PJM 11/12/99
2	CHANGED PER DCR 991221-01	RWH 12/27/99 ECM 1/4/00	CW 1/5/00 PJM 1/5/00
3	REVERSED J21 POLARITY, CHGD INVERTER ON/OFF CIRCUIT, CHGD R138 VALUE PER ECO 000217-00 & A	RWH 3/10/00 ECM 3/10/00	CW 3/10/00 PJM 3/10/00

CONTRACT NO.

lexicon
3 OAK PARK
BEDFORD, MA 01730

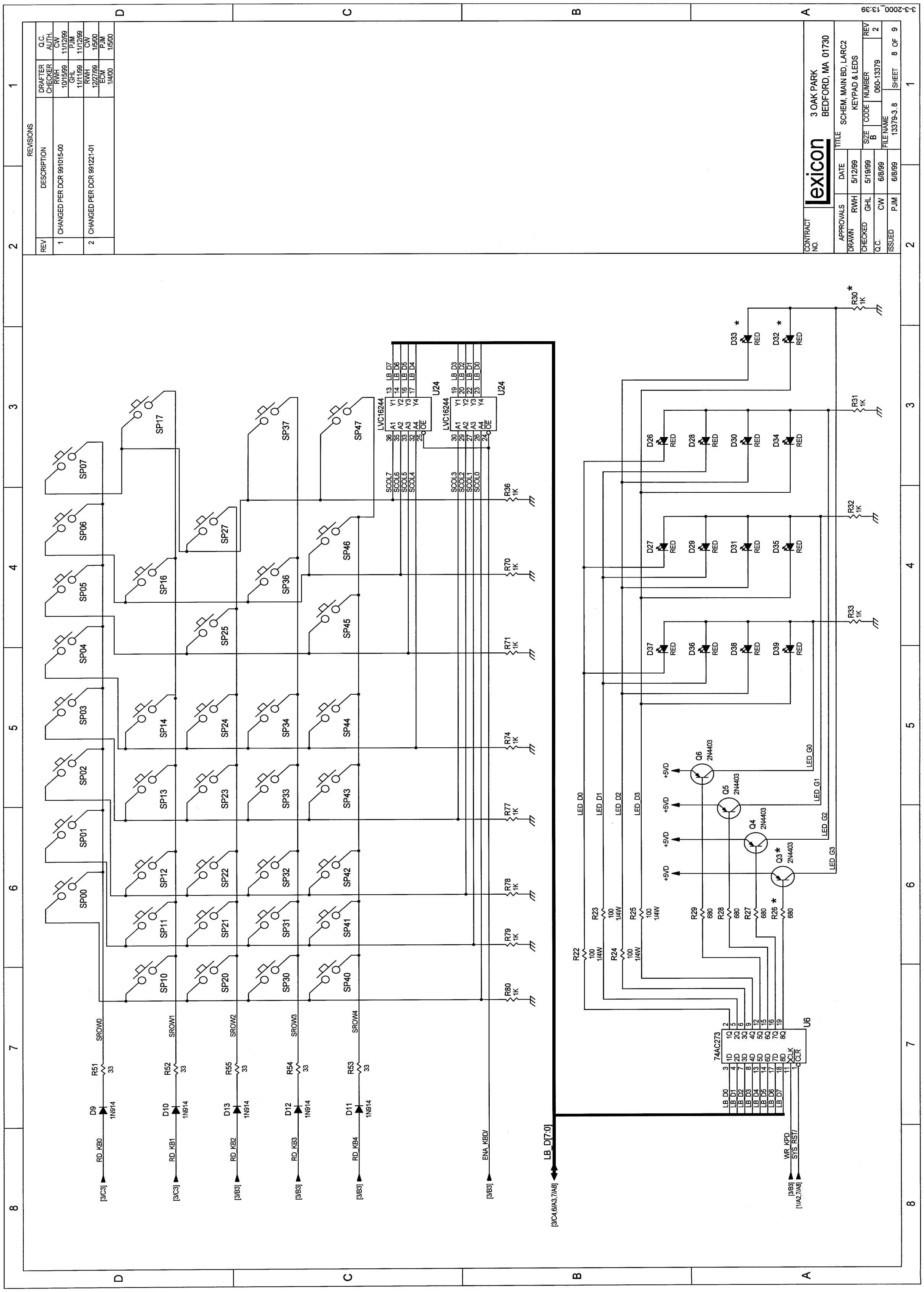
APPROVALS		DATE
DRAWN	RWH	5/12/99
CHECKED	GHL	5/19/99
Q.C.	CW	6/8/99
ISSUED	PJM	6/8/99

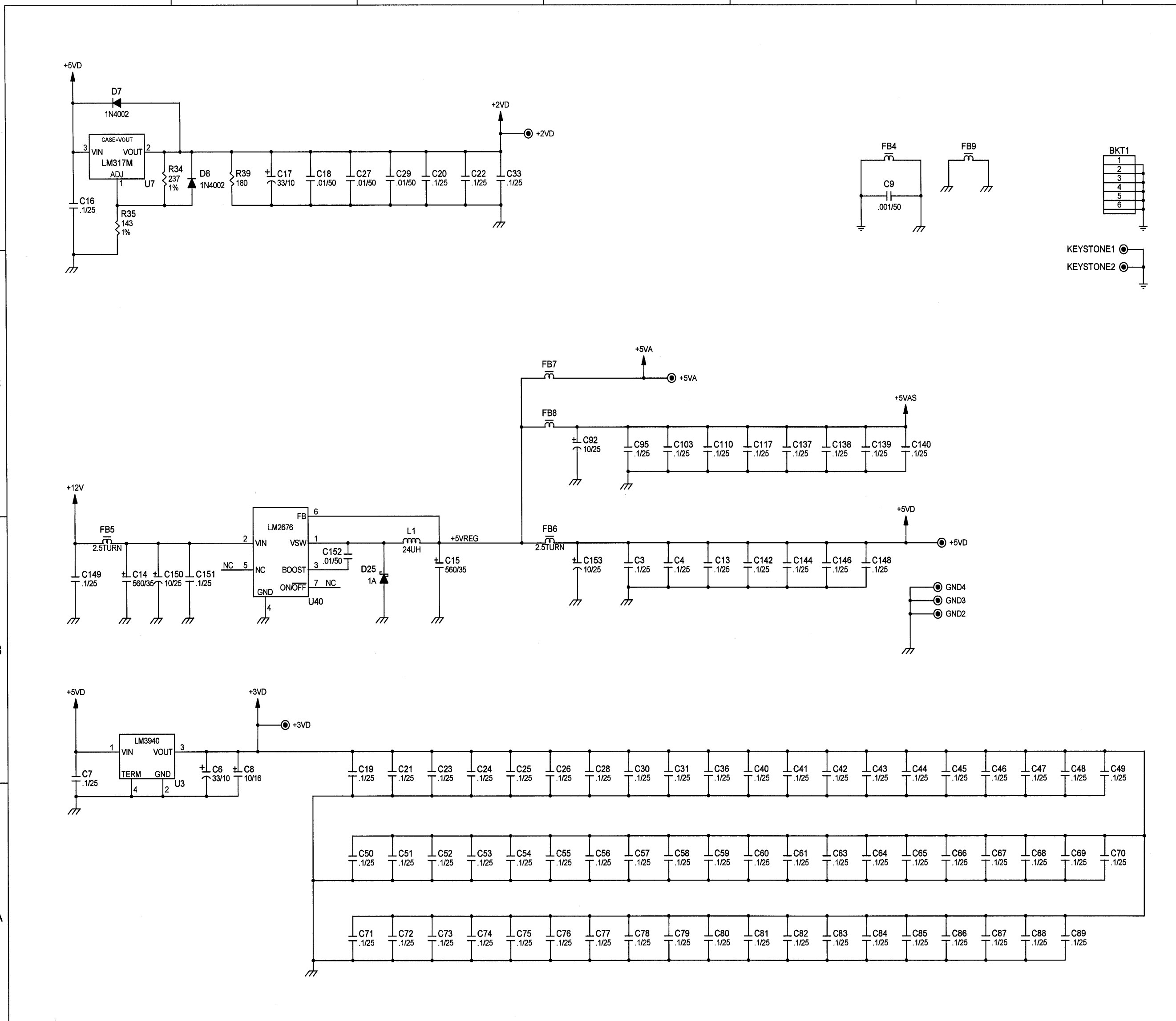
TITLE SCHEM, MAIN BD, LARC2 CONNECTORS & INDICATORS

SIZE B | CODE | NUMBER 060-13379 | REV 3

FILE NAME 13379-3.7 | SHEET 7 OF 9

3-14-2000_9:55


lexicon
3 OAK PARK
BEDFORD, MA 01730
SCHEM, MAIN BD, LARC2
KEYPAD & LEDS
060-13379
SHEET 8 OF 9
LVC16244
74AC273
LB_D[7:0]



REVISIONS

REV	DESCRIPTION	DRAFTER CHECKER	Q.C. AUTH.
1	CHANGED PER DCR 991015-00	RWH 10/15/99 GHL 11/11/99	CW 11/12/99 PJM 11/12/99
2	CHANGED PER DCR 991221-01	RWH 12/27/99 ECM 1/4/00	CW 1/5/00 PJM 1/5/00

CONTRACT NO.

lexicon 3 OAK PARK BEDFORD, MA 01730

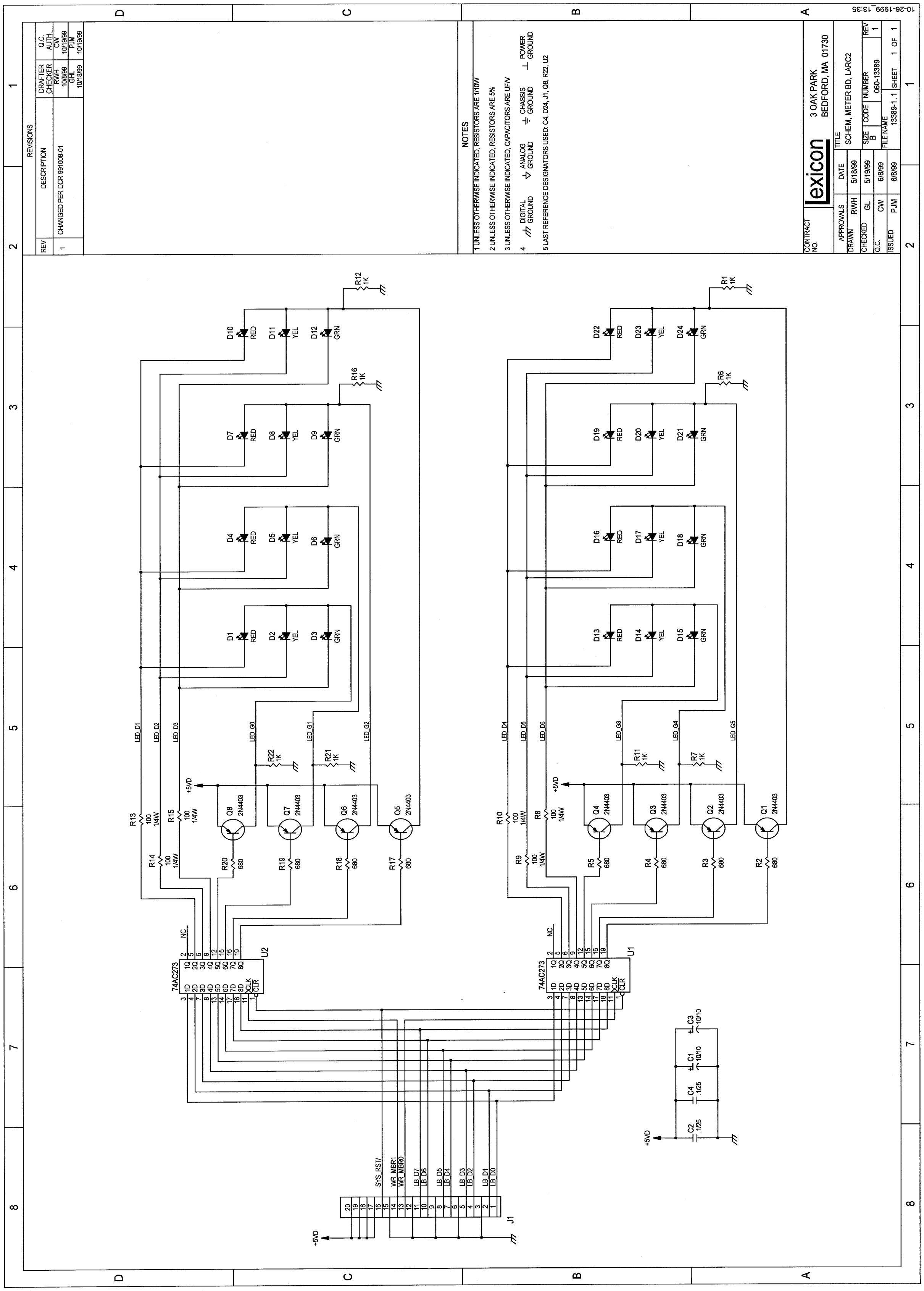
APPROVALS		DATE
DRAWN	RWH	5/12/99
CHECKED	GHL	5/19/99
Q.C.	CW	6/8/99
ISSUED	PJM	6/8/99

TITLE SCHEM, MAIN BD, LARC2 POWER SUPPLY & BYPASS CAPS

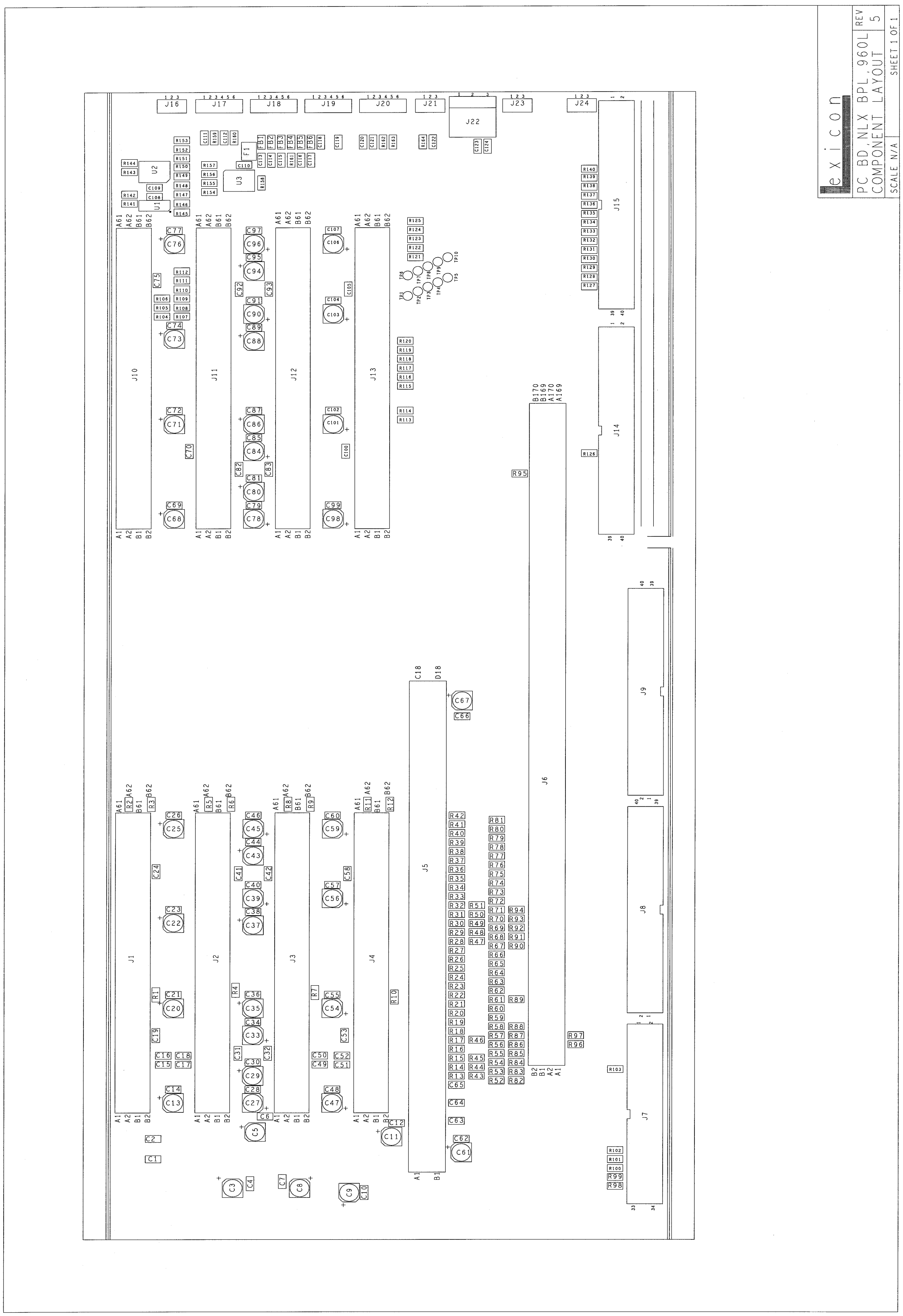
SIZE B | CODE | NUMBER 060-13379 | REV 2

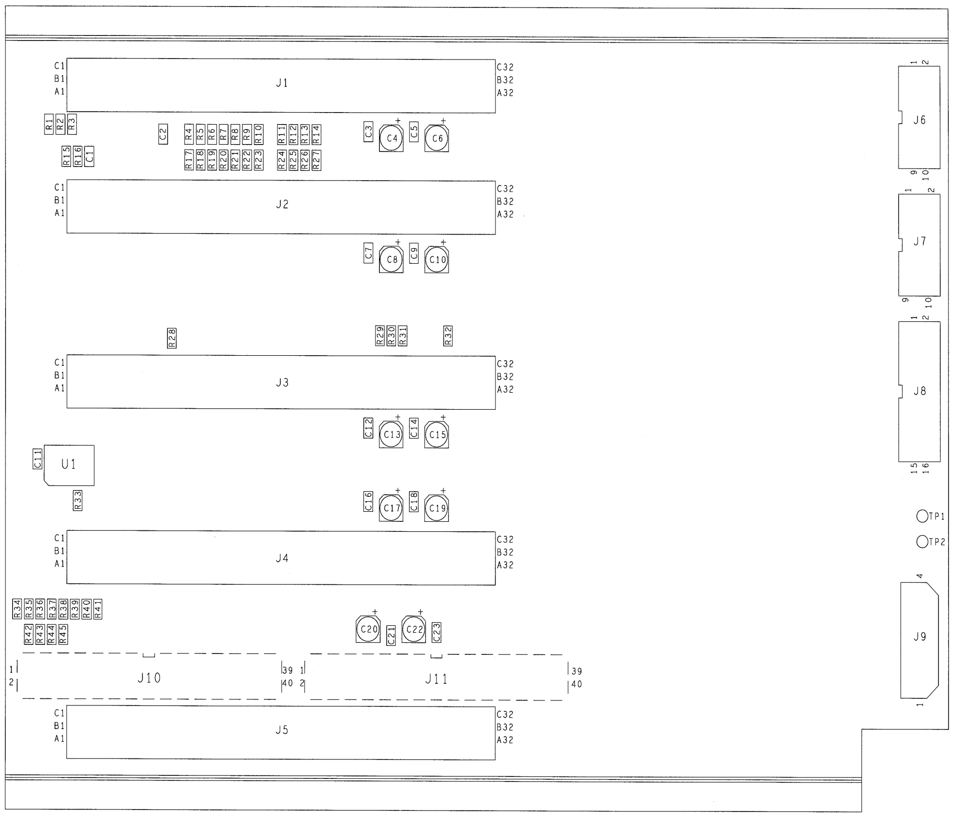
FILE NAME 13379-3.9 | SHEET 9 OF 9

3-3-2000_13:36


REVISIONS
REV | DESCRIPTION | DRAFTER CHECKER | Q.C. AUTH.
1 | CHANGED PER DCR 991008-01 | RWH 10/8/99 GHL 10/18/99 | CW 10/19/99 PJM 10/19/99
NOTES
1 UNLESS OTHERWISE INDICATED, RESISTORS ARE 1/10W
2 UNLESS OTHERWISE INDICATED, RESISTORS ARE 5%
3 UNLESS OTHERWISE INDICATED, CAPACITORS ARE UF/V
4 DIGITAL GROUND ANALOG GROUND CHASSIS GROUND POWER GROUND
5 LAST REFERENCE DESIGNATORS USED: C4, D24, J1, Q8, R22, U2
lexicon
3 OAK PARK
BEDFORD, MA 01730
TITLE
SCHEM, METER BD, LARC2
SIZE B
NUMBER 060-13389
REV 1
FILE NAME 13389-1.1
SHEET 1 OF 1
DRAWN RWH 5/18/99
CHECKED GL 5/19/99
Q.C. CW 6/8/99
ISSUED PJM 6/8/99
10-26-1999_13:35

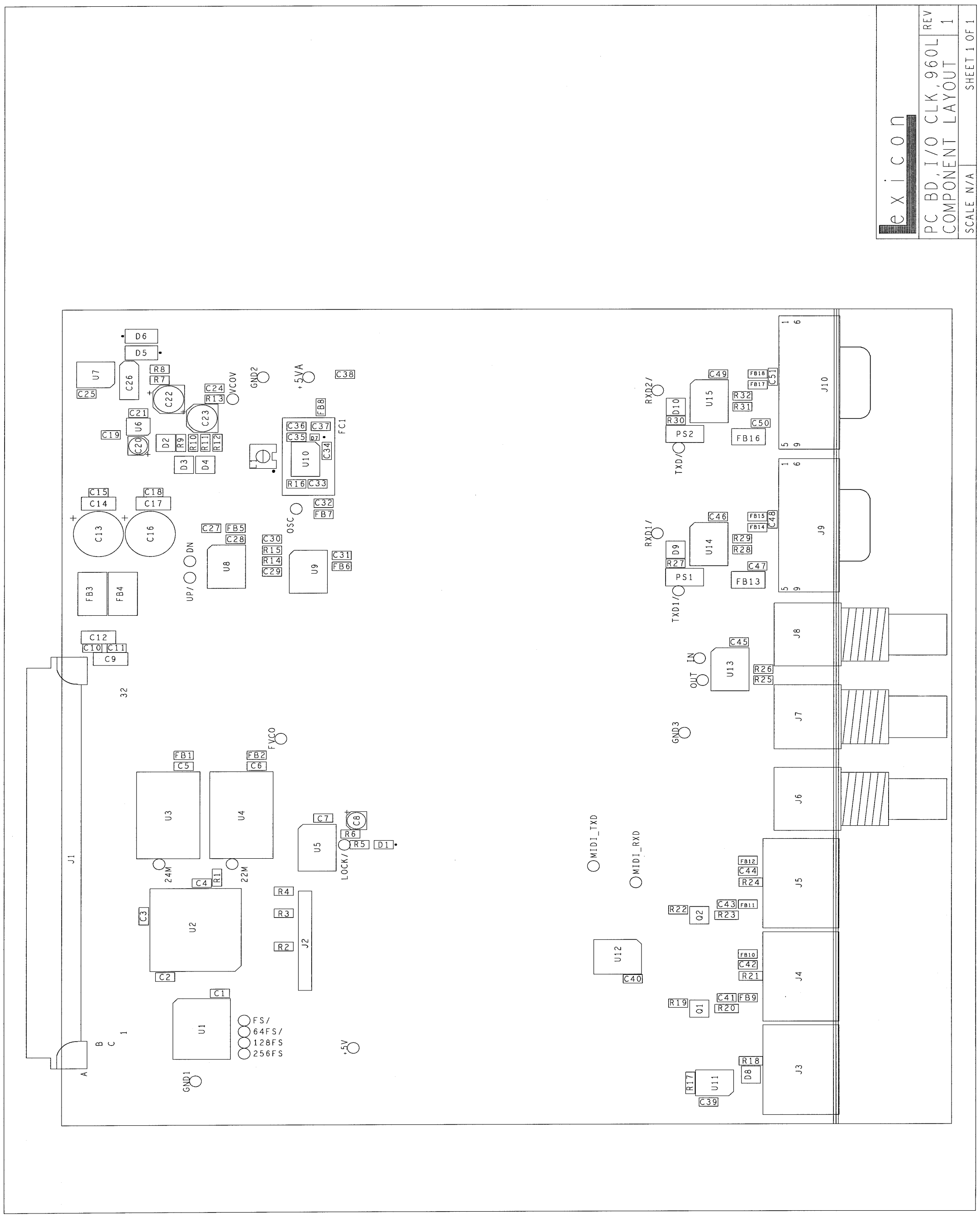
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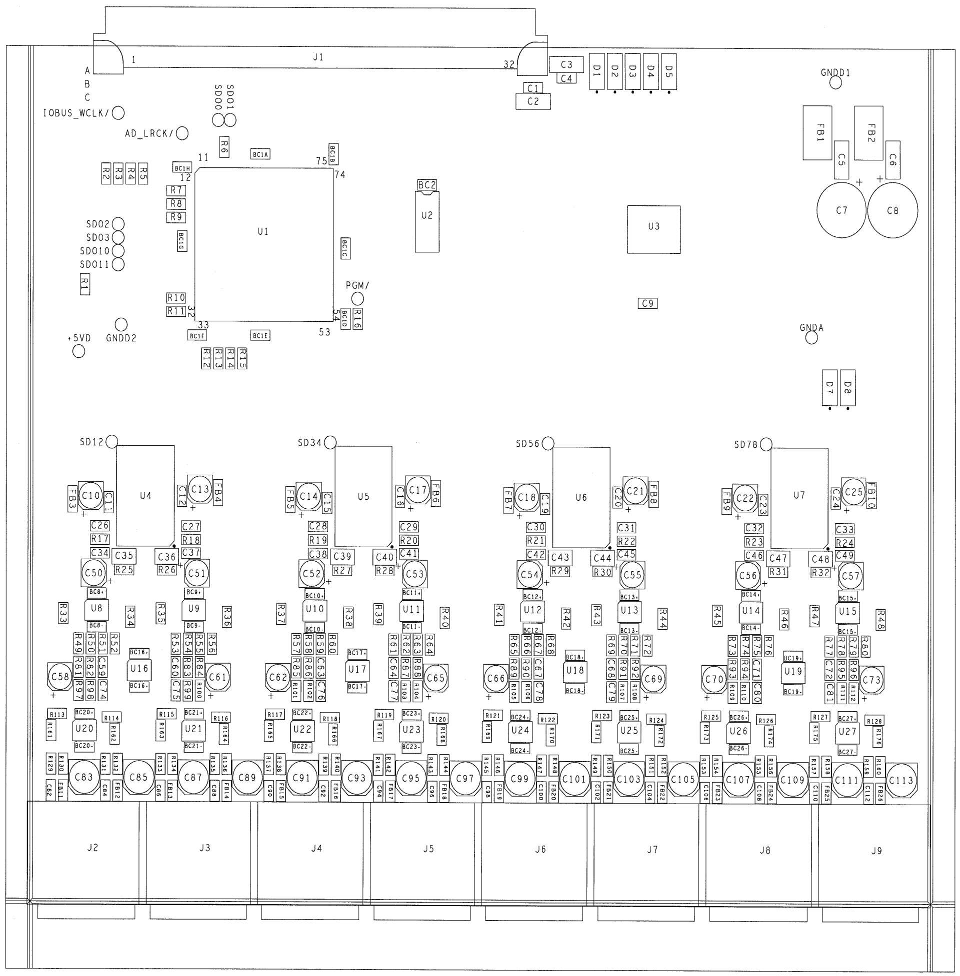

lexicon
PC BD, NLX BPL 960L
COMPONENT LAYOUT
REV 5
SCALE N/A
SHEET 1 OF 1



Lexicon

PC BD, I/O BPL, 960L COMPONENT LAYOUT	REV 3
SCALE N/A	SHEET 1 OF 1


lexicon
PC BD, I/O CLK, 960L
COMPONENT LAYOUT
REV
1
SCALE N/A
SHEET 1 OF 1



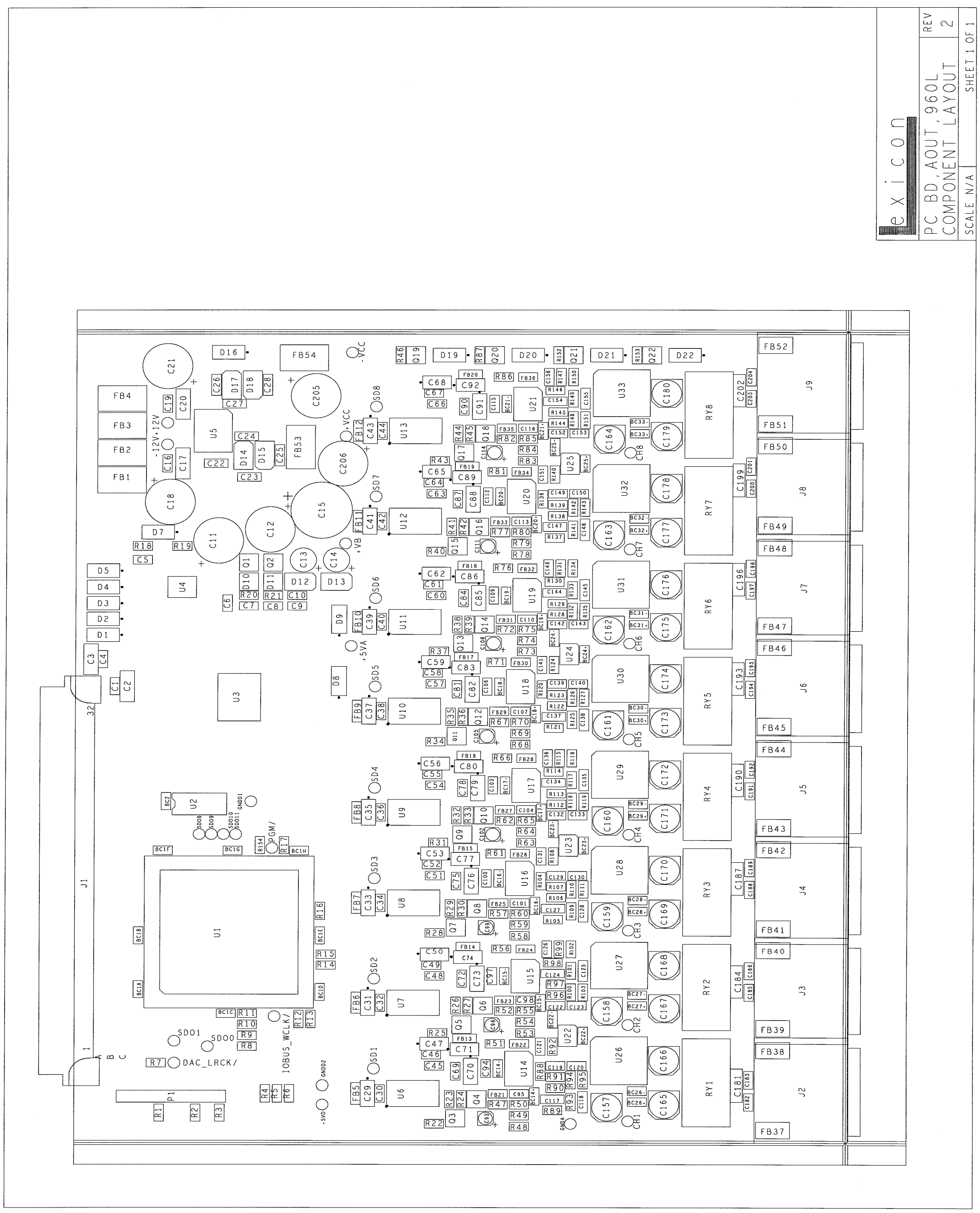
lexicon

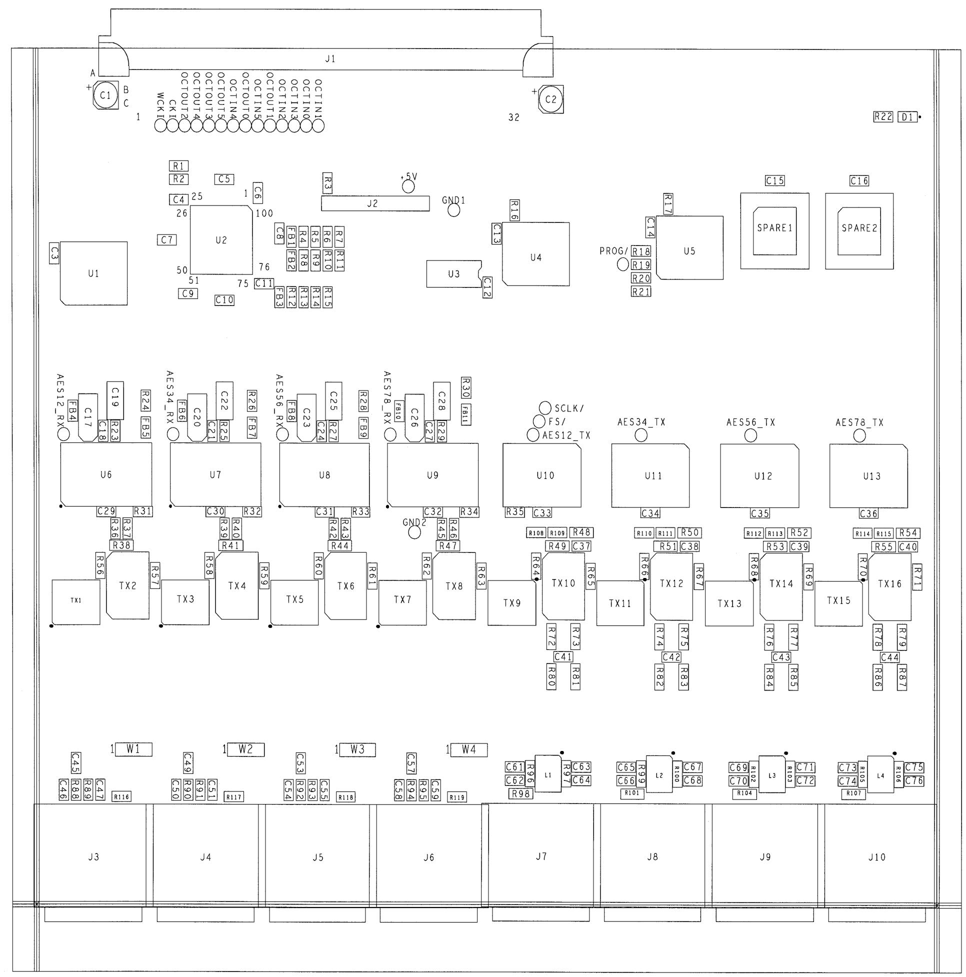
PC BD, AIN, 960L
COMPONENT LAYOUT

REV 3

SCALE N/A

SHEET 1 OF 1


lexicon
PC BD, AOUT, 960L
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 1 OF 1



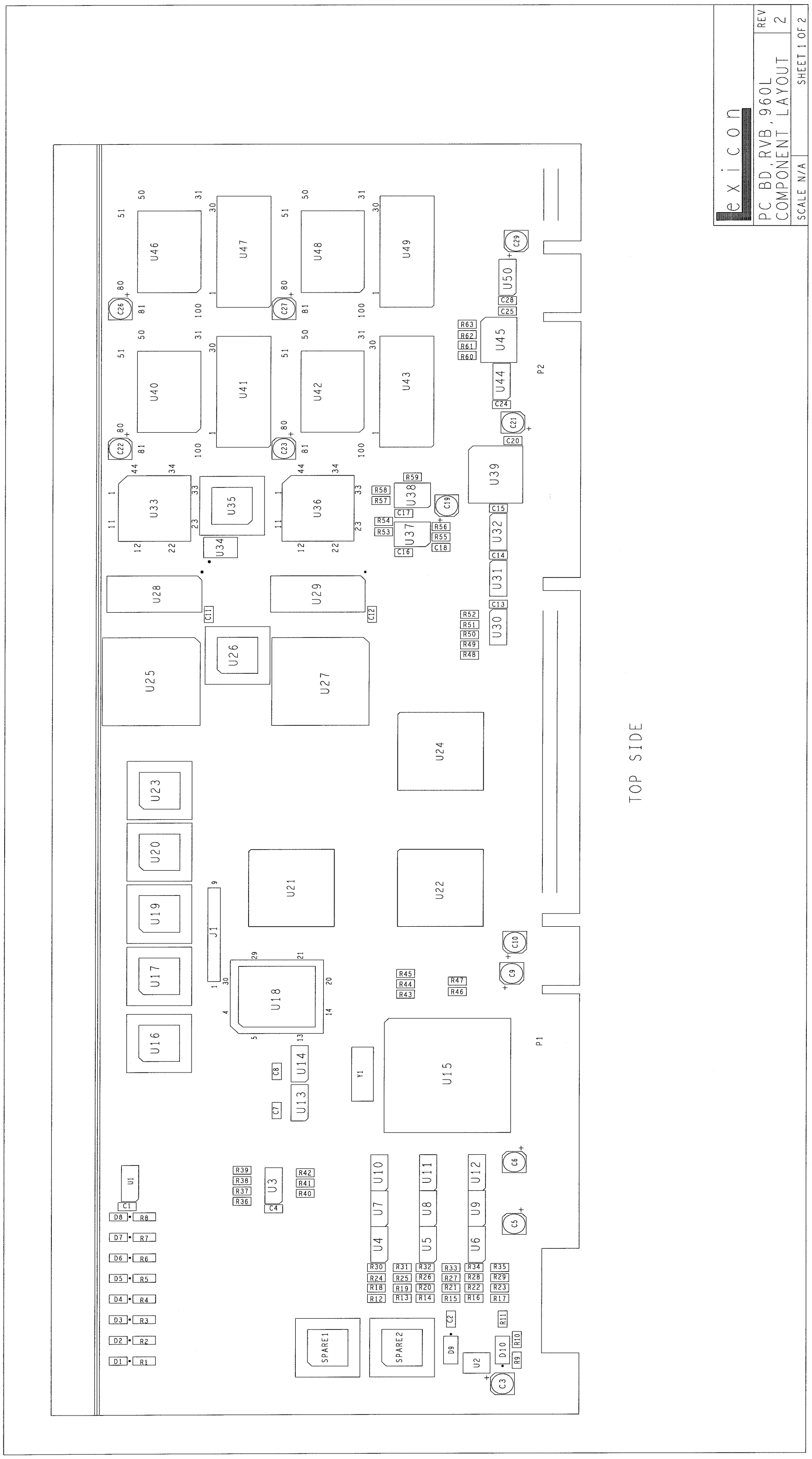
lexicon

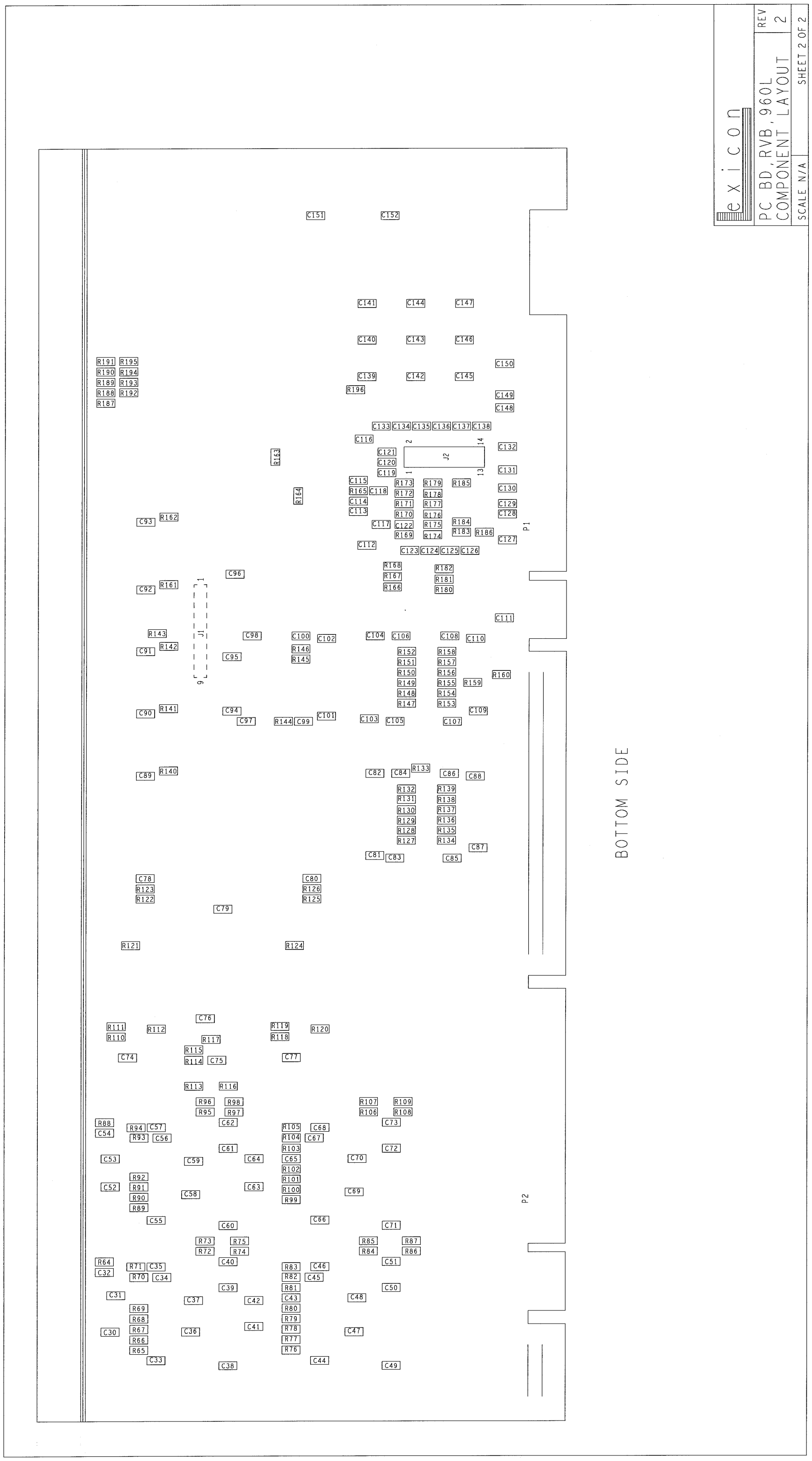
PC BD,AES,960L
COMPONENT LAYOUT

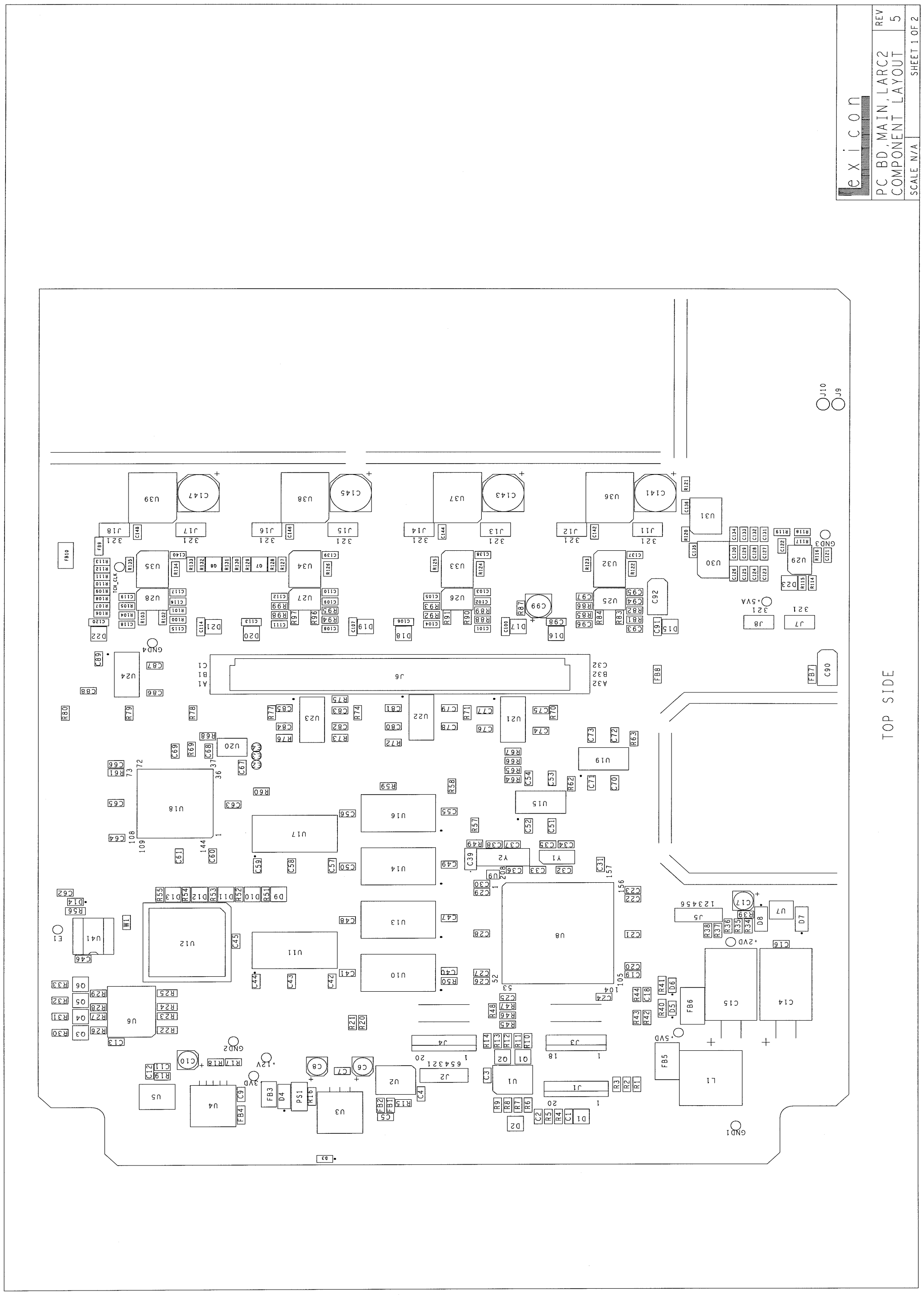
REV 2

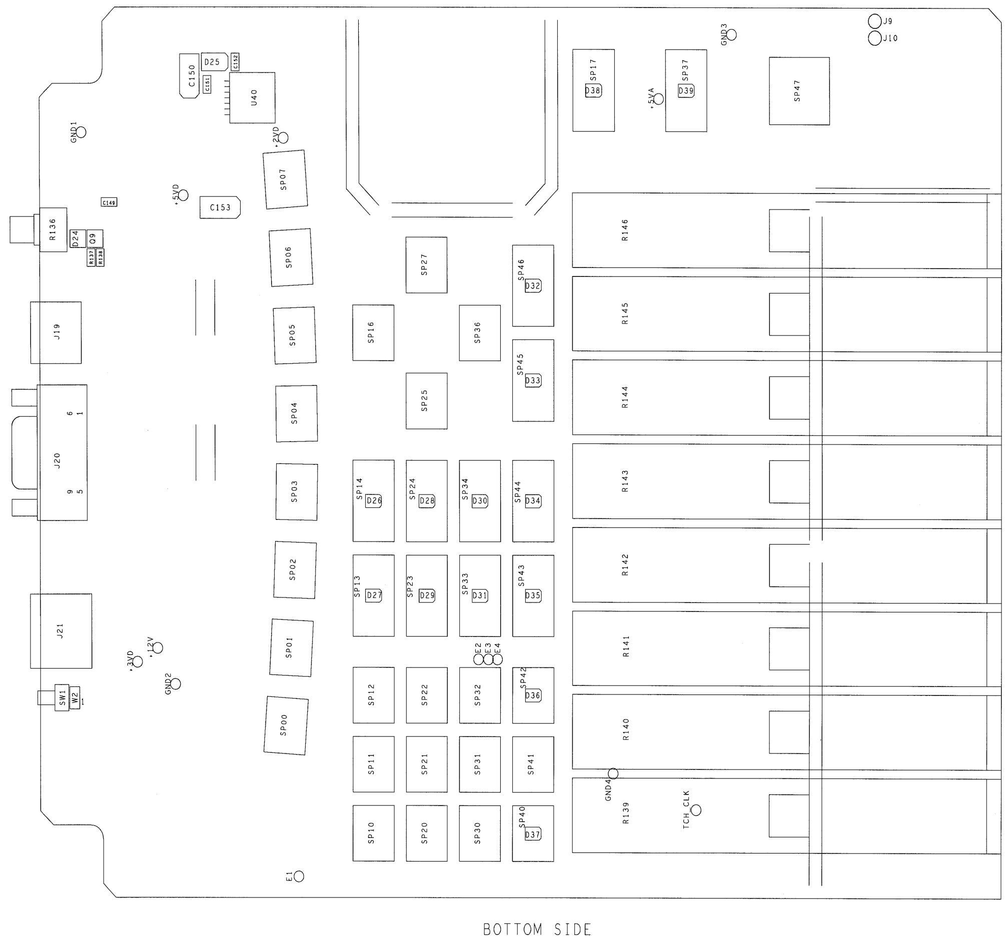
SCALE N/A

SHEET 1 OF 1


lexicon
PC BD, RVB, 960L
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 1 OF 2
TOP SIDE

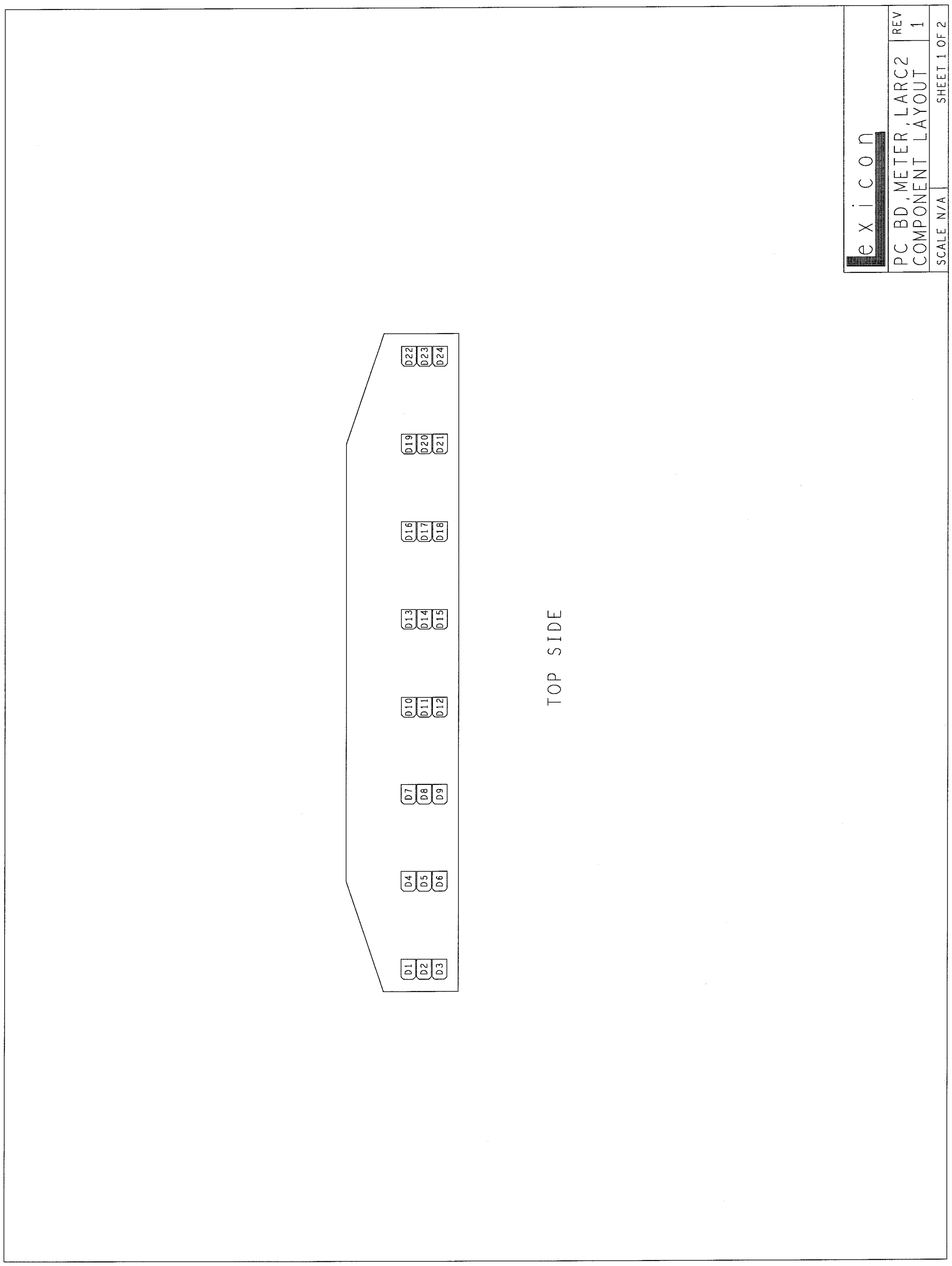

exicon
PC BD, RVB, 960L
COMPONENT LAYOUT
REV
2
SCALE N/A
SHEET 2 OF 2
BOTTOM SIDE
P1
P2
J1
J2

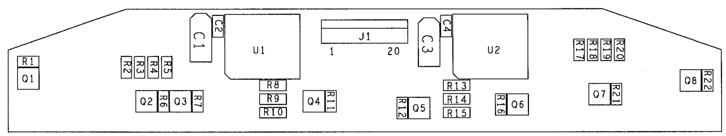

lexicon
PC BD, MAIN, LARC2
COMPONENT LAYOUT
REV
5
SCALE N/A
SHEET 1 OF 2
TOP SIDE



lexicon

PC BD, MAIN, LARC2 COMPONENT LAYOUT	REV 5
SCALE N/A	SHEET 2 OF 2


lexicon
PC BD, METER, LARC2
COMPONENT LAYOUT
REV
1
SCALE N/A
SHEET 1 OF 2
TOP SIDE
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
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D24



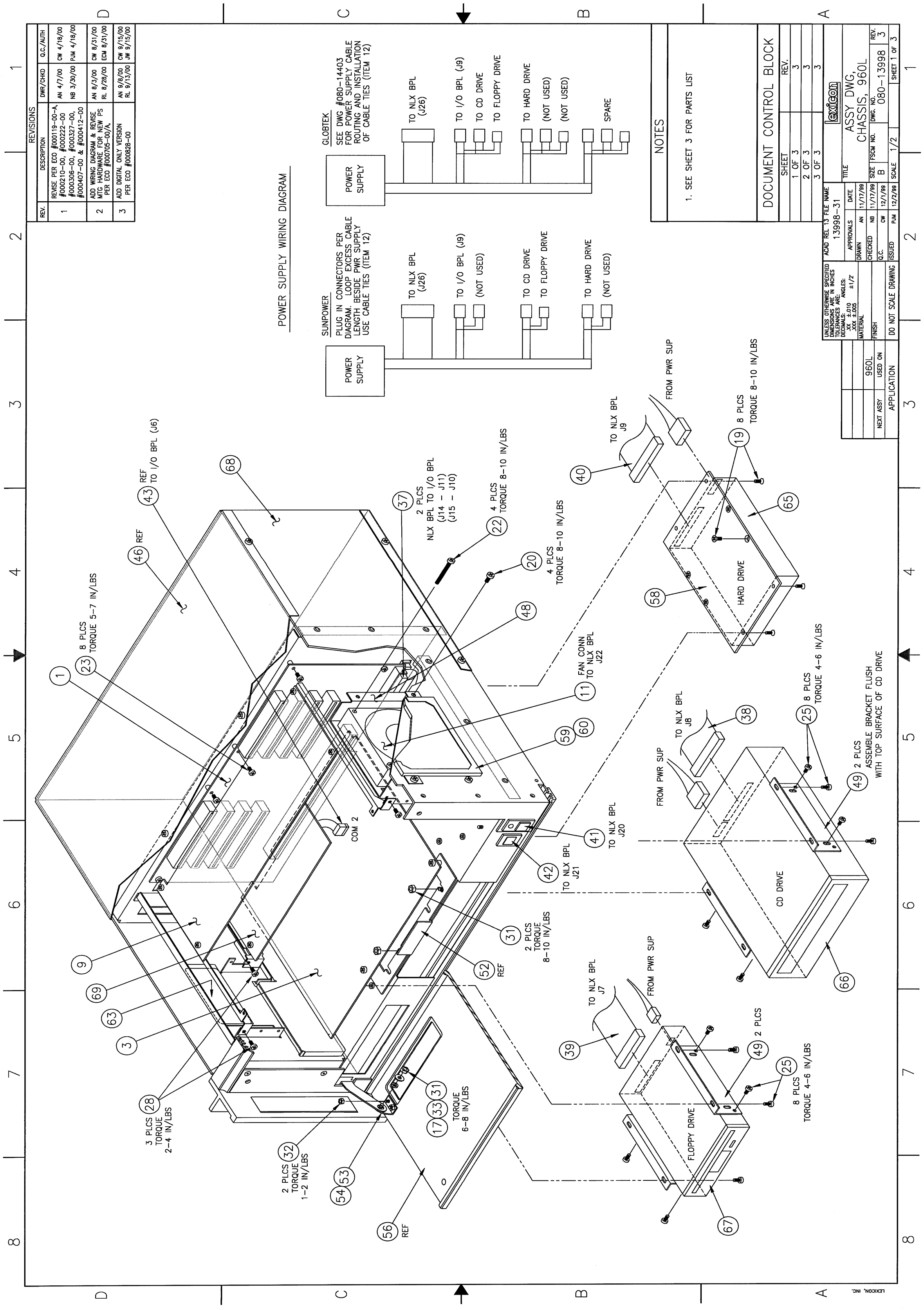
BOTTOM SIDE

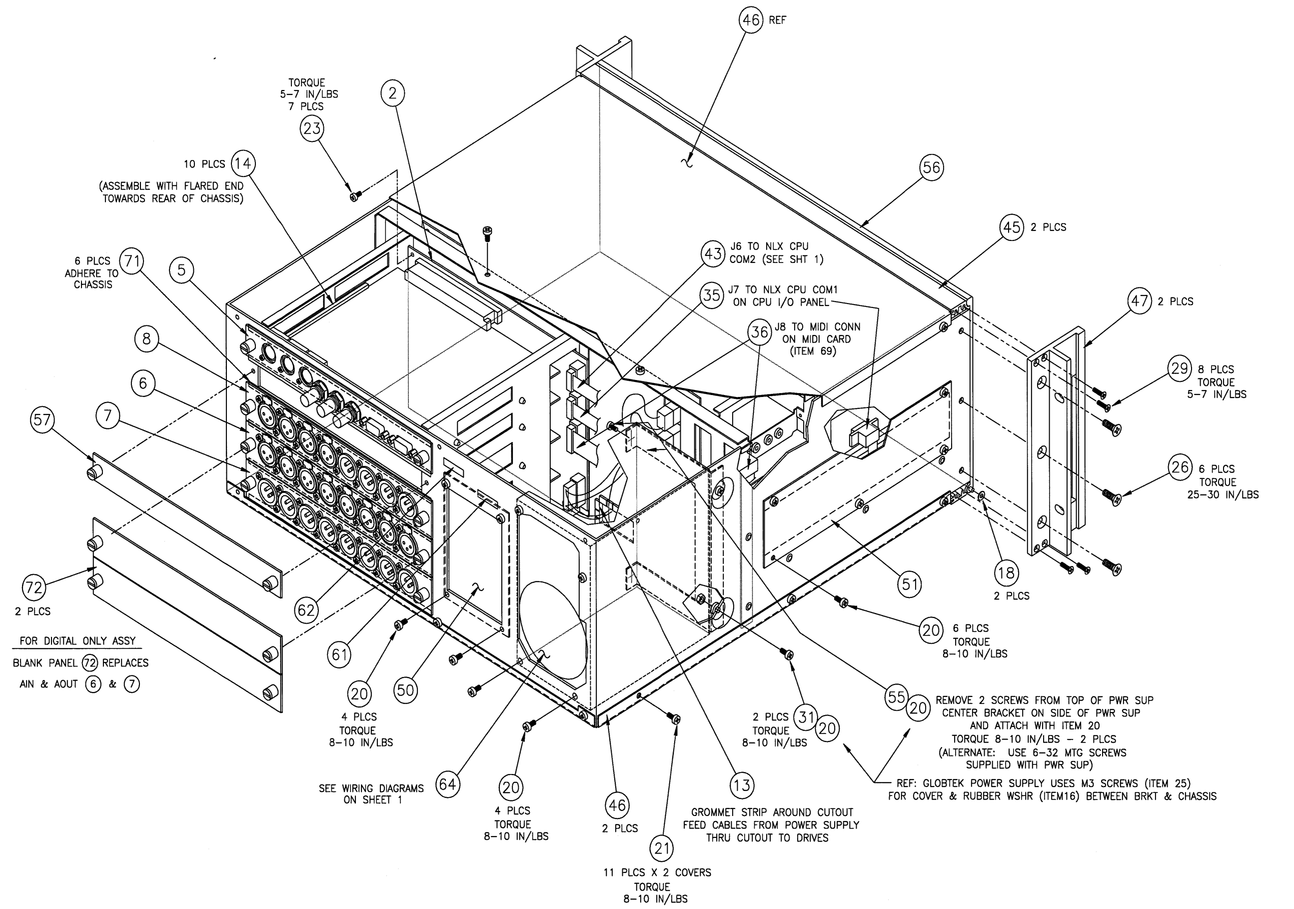
lexicon

PC BD, METER, LARC2 COMPONENT LAYOUT	REV 1
SCALE N/A	SHEET 2 OF 2

Your Notes:

Your Notes:


REVISIONS
POWER SUPPLY WIRING DIAGRAM
SUNPOWER
PLUG IN CONNECTORS PER DIAGRAM. LOOP EXCESS CABLE LENGTH BESIDE PWR SUPPLY USE CABLE TIES (ITEM 12)
GLOBTEK
SEE DWG #080-14403 FOR POWER SUPPLY CABLE ROUTING AND INSTALLATION OF CABLE TIES (ITEM 12)
POWER SUPPLY
TO NLX BPL (J26)
TO I/O BPL (J9)
TO CD DRIVE
TO FLOPPY DRIVE
TO HARD DRIVE
(NOT USED)
SPARE
NOTES
1. SEE SHEET 3 FOR PARTS LIST
DOCUMENT CONTROL BLOCK
ASSY DWG, CHASSIS, 960L
080-13998
HARD DRIVE
CD DRIVE
FLOPPY DRIVE
COM 2
FROM PWR SUP
8 PLCS TORQUE 5-7 IN/LBS
4 PLCS TORQUE 8-10 IN/LBS
8 PLCS TORQUE 4-6 IN/LBS
2 PLCS ASSEMBLE BRACKET FLUSH WITH TOP SURFACE OF CD DRIVE



REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD 55 & 29 PER ECO #000119-00-A; ADD 64 & NOTE AT 14 PER ECO#000210-00; ADD 71 PER ECO#000327-00; CHG 34 TO 18 PER ECO#000407-00; REVERSE POSITIONS OF MODULES 6 & 7 PER ECO#000412-00	AN 4/7/00 NB 3/30/00	CW 4/18/00 FJM 4/18/00
2	REVISE PWR SUP MTG HARDWARE PER ECO #000705-00/A	AN 8/17/00 RL 8/28/00	CW 8/31/00 ECM 8/31/00
3	ADD 72 FOR DIGITAL ONLY ASSY PER ECO #000828-00	AN 9/8/00 RL 9/13/00	CW 9/15/00 JW 9/15/00

NOTES

NEXT ASSY	USED ON
	960L
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 13998-32

APPROVALS		DATE
DRAWN	AN	11/17/99
CHECKED	NB	11/17/99
Q.C.	CW	12/1/99
ISSUED	FJM	12/2/99

lexicon

TITLE ASSY DWG, CHASSIS, 960L

SIZE B | FSCM NO. | DWG. NO. 080-13998 | REV. 3

SCALE 1/2 | SHEET 2 OF 3

LEXICON, INC.

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
1.	023-14012	PL, NLX BPL ASSY	1	
2.	023-14013	PL, I/O BPL ASSY	1	
3.	023-14019	PL, NLX CPU BD ASSY	1	
4.				
5.	023-14014	PL, I/O CLK BD ASSY	1	
6.	023-14015	PL, ANALOG IN BD ASSY	1	(NOT USED ON DIGITAL ONLY ASSY)
7.	023-14016	PL, ANALOG OUT BD ASSY	1	(NOT USED ON DIGITAL ONLY ASSY)
8.	023-14017	PL, AES BD ASSY	1	
9.	023-14018	PL, RVB BD BD ASSY	1	
10.				
11.	022-14408	PL, FAN ASSY, 12VDC, 36CFM, W/CONN	1	
12.	530-02488	TIE, CABLE, NYL, .14"X5 5/8"	2	PS CABLE
13.	540-14303	GROMMET, STRIP, .037" GAP, NYL	4"	SUPPORT, CENTER
14.	600-13984	CARD GUIDE, 1/16 PCB, 4"L, 3" MTG	10	I/O CAGE
15.				
16.	630-14304	WSHR, FL, .170 ID X .375 OD X .093, RUB	REF	GLOBTEK PWR SUP TO CHASSIS
17.	630-14358	WSHR, FL, #6CL, 1/4 OD X 1/16, NYL	1	STOP TO STOP SUPPORT
18.	630-14514	WSHR, FL, #6CL, 1/4 OD X 1/32, BLKNYL	2	FRONT PANEL
19.	640-01711	SCRW, 6-32X1/4, FH, PH, ZN	8	PLATE TO HARD DRV & PAN
20.	640-01716	SCRW, 6-32X3/8, PNH, PH, ZN	22	PWR SUP TO CHASSIS (8) ACCESS PLATE TO CHASSIS (6) EXP PLATE TO CHASSIS (4) FAN SUPP BRKT TO CHASSIS (4)
21.	640-02704	SCRW, 6-32X1/4, PNH, PH, BLK	22	COVERS TO CHASSIS
22.	640-03675	SCRW, 6-32X1 1/4, PNH, PH, ZN	4	FAN TO FAN SUPPORT BRKT
23.	640-04339	SCRW, 4-40X1/4, PNH, PH, SEMS, ZN	15	I/O BPL TO CTR (7) NLX BPL TO CTR (8)
24.				
25.	640-10498	SCRW, M3X6MM, PNH, PH, BZ	16	BRKT TO DRIVES & PAN
26.	640-13996	SCRW, 10-32X1/2, PNH, PH, BZ	6	RACK MT TO CHASSIS
27.				
28.	641-01703	SCRW, TAP, AB, #4 X 1/4, PNH, PH, ZN	3	RVB BD MTG (2), MIDI BD MTG (1)
29.	641-13116	SCRW, TAP, AB, #4 X 3/8, FH, PH, BZ	8	RAILS TO RACK MT
30.				
31.	643-01728	NUT, 6-32, KEP, ZN	5	PWR SUP TO CHASSIS (2) NLX CPU TO BRKT (2) STOP TO STOP SUPPORT (1)
32.	643-08200	NUT, 4-40, HEX, ZN	2	STOP BRKT TO FP
33.	644-01735	WSHR, FL, #6 CL X 3/8 OD X 1/32 THK	1	STOP TO STOP SUPPORT
34.				
35.	680-13988	CABLE, RECP/DE9S, 9C, 18"L	1	NLX CPU TO I/O BPL
36.	680-13989	CABLE, RECP/DB15P, 15C, 18"L	1	MIDI BD TO I/O BPL
37.	680-13990	CABLE, .10, SCKT/SCKT, 2X20C, 2"L	2	I/O BPL TO NLX BPL
38.	680-13991	CABLE, .10, SCKT/SCKT, 2X20C, 6"L	1	CD ROM TO NLX BPL
39.	680-13992	CABLE, .10, SCKT/SCKT, 2X17C, 6"L	1	FLOPPY DR TO NLX BPL
40.	680-14203	CABLE, .10, SCKT/SCKT, 2X20C, 9"L	1	HARD DR TO NLX BPL
41.	680-14206	CABLE, .059, SCKT/SW&LED, 4C, 14"L	1	PWR SW TO NLX BPL
42.	680-14305	CABLE, .059, SCKT/SW, 3C, 14"L	1	RESET SW TO NLX BPL
43.	680-14306	CABLE, .10, SCKT/SCKT, 2X5C, 18"L	1	NLX CPU TO I/O BPL
44.				
45.	700-13965	RAIL, TOP/BOTTOM	2	
46.	700-13967	COVER, TOP/BOTTOM	2	
47.	701-13963	BRACKET, MTG, RACK, 4U	2	
48.	701-13968	BRACKET, SUPPORT, FAN	1	
49.	701-13969	BRACKET, SUPPORT, CD/DISK	4	
50.	701-13985	PLATE, EXPANSION, BLANK	1	
51.	701-13986	PLATE, ACCESS	1	
52.	701-14307	BRACKET, SUPPORT, NLX CPU	REF	
53.	701-14308	BRACKET, SUPPORT, STOP, FP	1	
54.	701-14309	STOP, FP	1	
55.	701-13346	BRACKET, NLX PS	1	

ITEM#	PART#	DESCRIPTION	QTY	WHERE USED
56.	702-13959	PANEL, FRONT	1	
57.	702-13972	PANEL, I/O, BLANK	1	
58.	702-13983	PLATE, MTG, HARD DRIVE	1	
59.	700-14406	FRAME, SUPPORT, AIR FILTER	1	
60.	720-14405	AIR FILTER, GRAY	1	
61.	740-09538	LABEL, S/N, CHASSIS	1	CHASSIS, REAR
62.	740-13573	LABEL, MFR ID	1	CHASSIS, REAR
63.	740-14348	LABEL, WINDOWS NT	1	SIDE SUPPORT
64.	750-13390	PWR SUPPLY	1	
65.	750-13391	HD DRIVE, BLANK (SEE BOM FOR PROG P/N)	1	
66.	750-13392	DRIVE, CD, IDE	1	
67.	750-13393	DRIVE, FLOPPY	1	
68.	750-13950	CHASSIS SUBASSY	1	
69.	750-14031	PCB ASSY, PCI MIDI	1	
70.				
71.	720-14404	GASKET, CONDFOAM, PSA	6	
72.	702-14518	PANEL, AUDIO, BLANK	2	DIGITAL ONLY (REPLACES AIN & AOUT)

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD (55), QTY CHG (25) PER ECO #000119-00-A; ADD (34), QTY CHG (21), CHG (52) TO REF, P/N CHG (65) PER ECO #000210-00; ADD (63) PER ECO #000222-00; ADD (11), (22), (59) & (60) PER ECO #000306-00; ADD (12) & (71) PER ECO #000327-00; DELETE (34), ADD (18) PER ECO #000407-00	AN 4/7/00 NB 3/30/00	CW 4/18/00 PJM 4/18/00
2	CHG (16) TO REF, CHG QTY: (12), (20) & (25) PER ECO #000705-00/A	AN 8/17/00 RL 8/28/00	CW 8/31/00 ECM 8/31/00
3	ADD (72) (BLANK AUDIO PANEL) FOR DIGITAL ONLY ASSY PER ECO #000828-00	AN 9/8/00 RL 9/13/00	CW 9/15/00 JW 9/15/00

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY AND DOES NOT SUPERSEDE THE BILL OF MATERIAL:
   #022-14010
   #022-14809 (DIGITAL ONLY)

NEXT ASSY	USED ON
	960L

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 13998-33

APPROVALS		DATE
DRAWN	AN	11/16/99
CHECKED	NB	11/17/99
Q.C.	CW	12/1/99
ISSUED	PJM	12/2/99

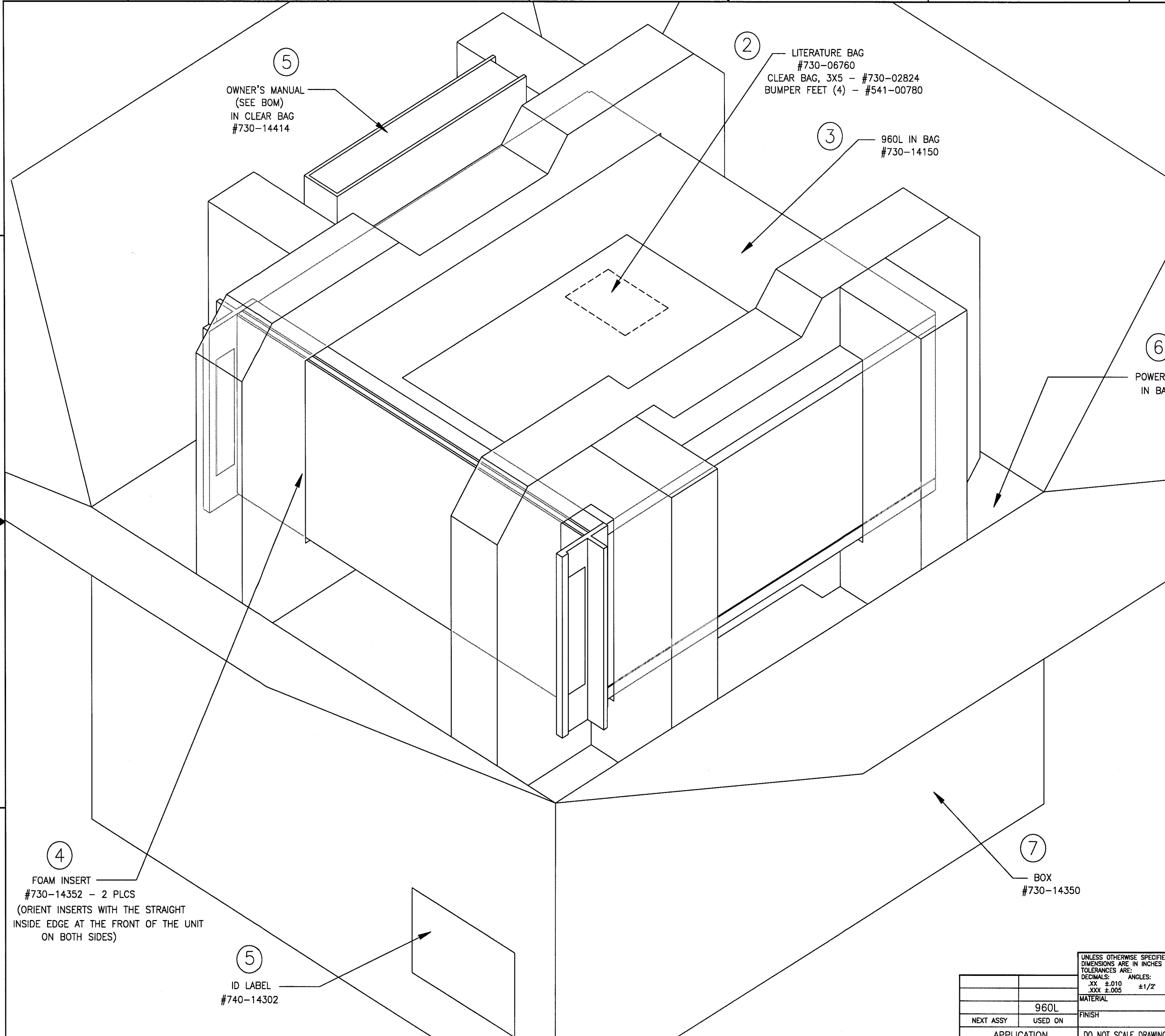
lexicon

TITLE ASSY DWG, CHASSIS, 960L

SIZE B | FSCM NO. | DWG. NO. 080-13998 | REV. 3

SCALE NONE | SHEET 3 OF 3

LEXICON, INC.



REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD BAG FOR PWR CORD, CHG FEET P/N, REVISE NOTES PER ECO #000222-00	AN 3/2/00 NB 3/3/00	CW 3/3/00 PJM 3/3/00
2	ADD REF FOR DIGITAL ONLY BOM TO NOTE 1 PER ECO #000828-00	AN 9/8/00 RL 9/13/00	CW 9/15/00 JW 9/15/00

NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOM #022-14008 OR #022-14808 (DIGITAL ONLY)
2. LITERATURE AND OTHER ITEMS SPECIFIED ON BOM ARE TO BE STACKED IN ORDER OF SIZE, WITH SMALLER ITEMS ON TOP, AND PLACED IN BAG. PUT BUMPER FEET (4) IN SMALL BAG AND PLACE IN LARGE BAG WITH LITERATURE. HEAT SEAL BAG AND TAPE TO TOP OF UNIT.
3. PLACE UNIT IN BAG. FOLD AND TAPE BAG WITH CREASES AND TAPE ON BOTTOM SIDE OF UNIT. USE CLEAR TAPE.
4. PUT FOAM INSERTS ON UNIT (NOTE ORIENTATION) AND PLACE IN BOX.
5. PUT OWNER'S MANUAL IN BAG, HEAT SEAL, PLACE BETWEEN FOAM STRUTS ON LEFT SIDE OF BOX.
6. PUT APPROPRIATE POWER CORD (SEE BOM) IN SELF-SEALING CUSHIONED BAG. PLACE IN RIGHT REAR CORNER OF BOX.
7. CLOSE BOX FLAPS AND TAPE.
8. ADD ID LABEL TO BOX IN SPACE PROVIDED

960L	
USED ON	NEXT ASSY
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 13999-2

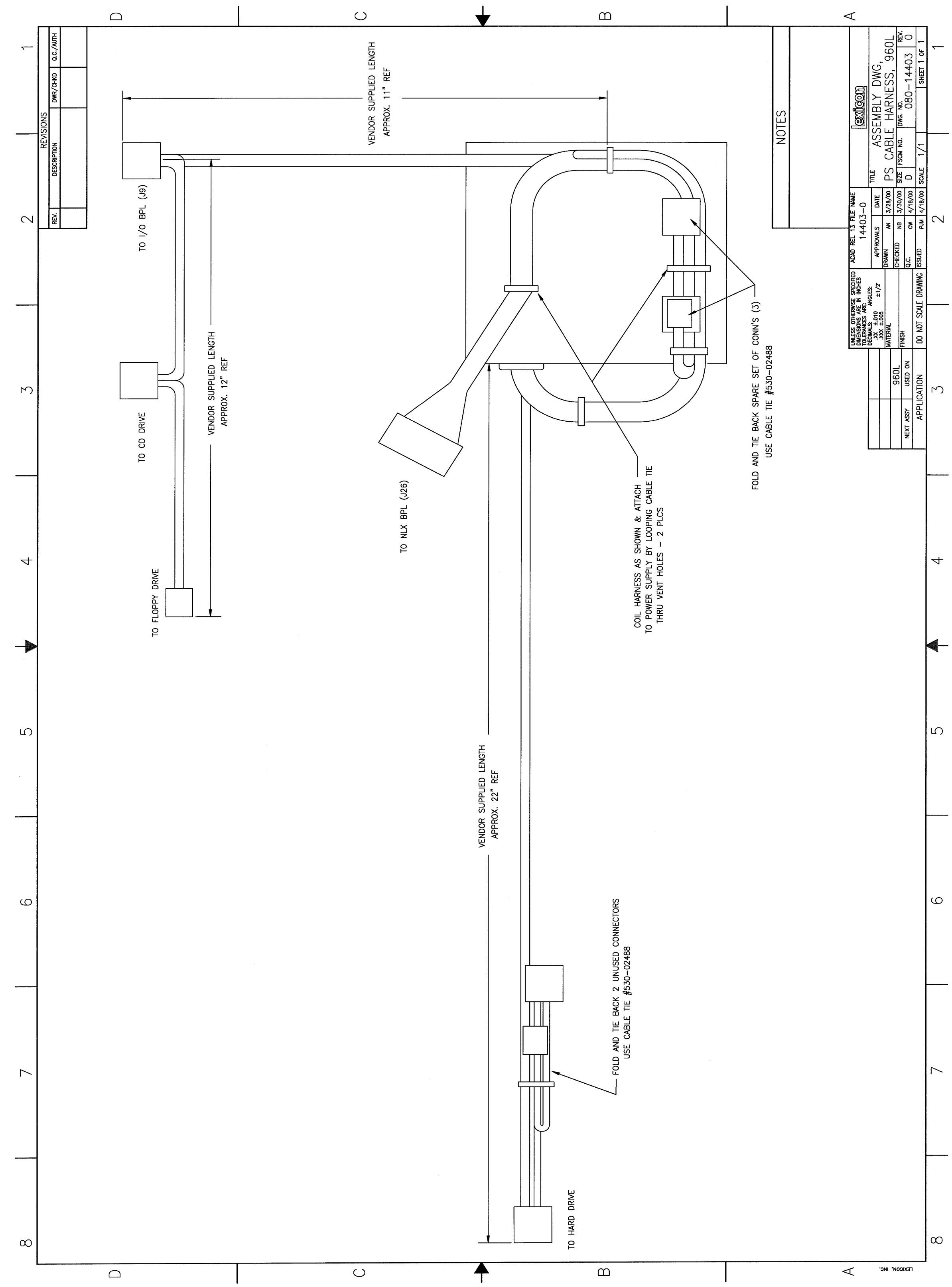
APPROVALS		DATE
DRAWN	AN	11/8/99
CHECKED	NB	11/17/99
Q.C.	CW	12/1/99
ISSUED	PJM	12/2/99

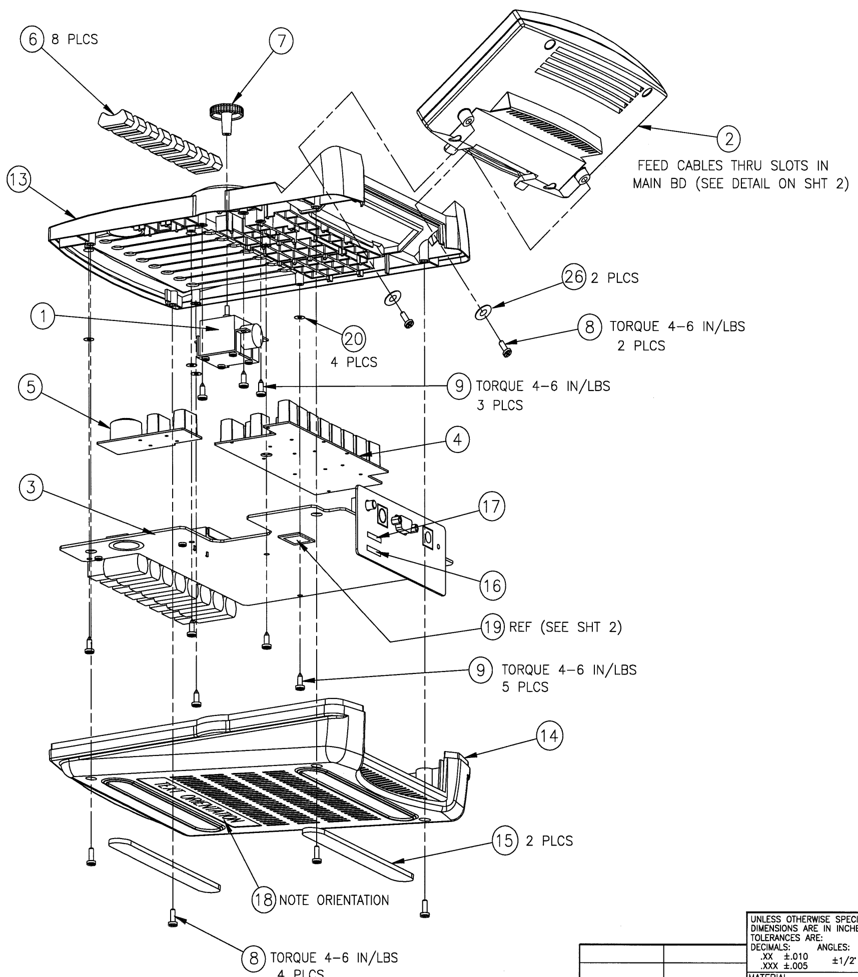
lexicon

TITLE ASSY DWG, SHIPMENT, 960L

SIZE B | FSCM NO. | DWG. NO. 080-13999 | REV. 2
SCALE 1/4 | SHEET 1 OF 1

LEXICON, INC.


REVISIONS
REV.
DESCRIPTION
DWR/CHKD
Q.C./AUTH
NOTES
VENDOR SUPPLIED LENGTH
APPROX. 11" REF
VENDOR SUPPLIED LENGTH
APPROX. 12" REF
VENDOR SUPPLIED LENGTH
APPROX. 22" REF
TO I/O BPL (J9)
TO CD DRIVE
TO FLOPPY DRIVE
TO NLX BPL (J26)
TO HARD DRIVE
COIL HARNESS AS SHOWN & ATTACH
TO POWER SUPPLY BY LOOPING CABLE TIE
THRU VENT HOLES - 2 PLCS
FOLD AND TIE BACK SPARE SET OF CONN'S (3)
USE CABLE TIE #530-02488
FOLD AND TIE BACK 2 UNUSED CONNECTORS
USE CABLE TIE #530-02488
ACAD REL 13 FILE NAME
14403-0
TITLE
ASSEMBLY DWG,
PS CABLE HARNESS, 960L
SIZE
D
DWG. NO.
080-14403
REV.
0
SCALE 1/1
SHEET 1 OF 1
APPROVALS
DATE
DRAWN AN 3/28/00
CHECKED NB 3/30/00
Q.C. CW 4/18/00
ISSUED PJM 4/18/00
DO NOT SCALE DRAWING
960L
NEXT ASSY
USED ON
APPLICATION
FINISH
MATERIAL
LEXICON, INC.



REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD ITEMS (20) & (21) PER ECO #000211-00	AN 2/15/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	ADD FERRITE (22), WASHER (26) PER ECO #000331-00/A CHG QTY (20) TO 4, DELETE (21) PER ECO #000419-00, CHG SHT 2 PER ECO #000425-00	AN 7/20/00 NB 7/28/00	CW 8/8/00 JW 8/9/00

NOTES

1. SEE SHEET 2 FOR PARTS LIST.

DOCUMENT CONTROL BLOCK

DOC. #	DESCRIPTION	REV.
080-14231	ASSY DWG, MAIN HSG SHT 1 OF 2	2
080-14231	ASSY DWG, MAIN HSG SHT 2 OF 2	2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

	LARC2
NEXT ASSY	USED ON
APPLICATION	

ACAD REL 13 FILE NAME: 14231-21

APPROVALS		DATE
DRAWN	JAM	9/8/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

lexicon

TITLE: ASSY DWG, MAIN HSG, LARC2

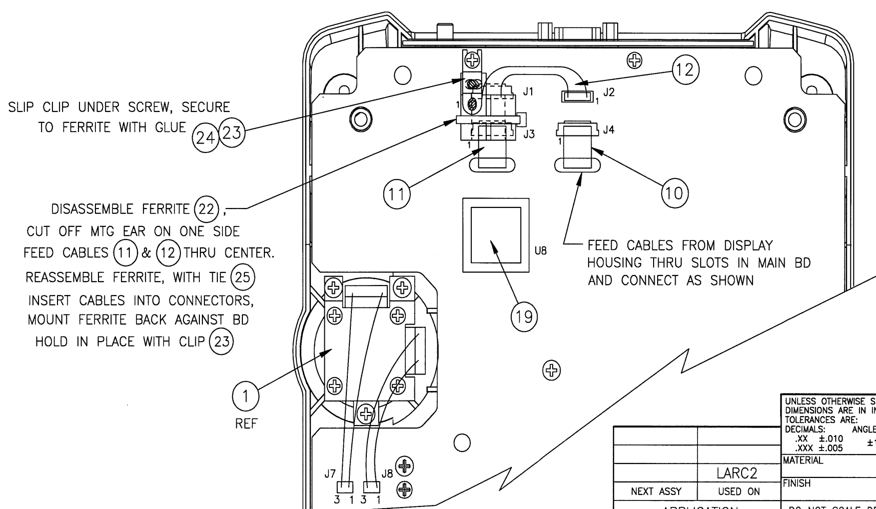
SIZE: B | FSCM NO. | DWG. NO.: 080-14231 | REV.: 2
SCALE: 1/1 | SHEET 1 OF 2

LEXICON, INC.

ITEM #	PART #	DESCRIPTION	QTY	WHERE USED
1.	022-14026	PL, JOYSTICK ASSY	1	
2.	022-14027	PL, DSPLY HSG ASSY	1	
3.	023-14022	PL, MAIN BD ASSY	1	
4.	453-14226	KEYPAD, MAIN	1	
5.	453-14228	KEYPAD, SIDE	1	
6.	550-14035	KNOB, SLIDE, TANG	8	FADERS
7.	550-14230	KNOB, JOYSTICK	1	
8.	640-01716	SCRW, 6-32X3/8, PNH, PH, ZN	6	DSPLY HSG TO MAIN HSG (2), TOP TO BOTTOM (4)
9.	641-01715	SCRW, TAP, AB, 6X3/8, PNH, PH, ZN	8	JOYSTICK ASSY TO TOP (3), MAIN BD TO TOP (5)
10.	680-14235	CABLE, FFC, 20CX.5MM, 7.5"	REF	METER BD TO MAIN BD
11.	680-14237	CABLE, FFC, 18CX.5MM, 5.7", FOLD	REF	LCD TO MAIN BD
12.	680-14238	CABLE, HSG/HSG, 5C/6C, 8.5"	REF	INVERTER TO MAIN BD
13.	700-14208	HOUSING, TOP	1	
14.	700-14211	HOUSING, BOTTOM	1	
15.	720-14223	PAD, FOOT	2	HSG, BOTTOM
16.	740-09538	LABEL, S/N, CHASSIS	1	REAR PANEL
17.	740-13573	LABEL, MFR, ID	1	REAR PANEL
18.	740-14200	LABEL, WARNINGS/APP	1	HSG, BOTTOM
19.	740-14349	LABEL, WINDOWS CE	1	MAIN BD (ON U8)
20.	630-12533	WSHR, FL, .120 IDX.25 ODX.062, RUB	4	MAIN BD TO TOP
21.				
22.	270-14401	FERRITE, FLAT CABLE, ~.8X1.2, HW	1	MAIN BD
23.	701-14517	CLIP, .78L X .28W X .29H, .100/.156	1	FERRITE TO MAIN BD
24.	120-14515	ADHESIVE, GLUE, HOT MELT, GP	1.135gr	CLIP TO FERRITE
25.	530-02489	TIE, CABLE, NYL, .1 X 4"	1	AROUND FERRITE
26.	644-06347	WSHR, FL, .195IDX.437ODX.030 THK, NYL	2	DSPLY HSG TO MAIN HSG

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	ADD ITEMS (20) & (21) PER ECO #000211-00	AN 2/15/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	ADD ITEMS (22) THRU (26) PER ECO #000331-00/A; CHG P/N & QTY ITEM (20), DELETE (21) PER ECO #000419-00; CHG P/N (23) PER ECO #000425-00	AN 7/20/00 NB 7/28/00	CW 8/8/00 JW 8/9/00



NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM #022-14021

	LARC2	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 14231-22

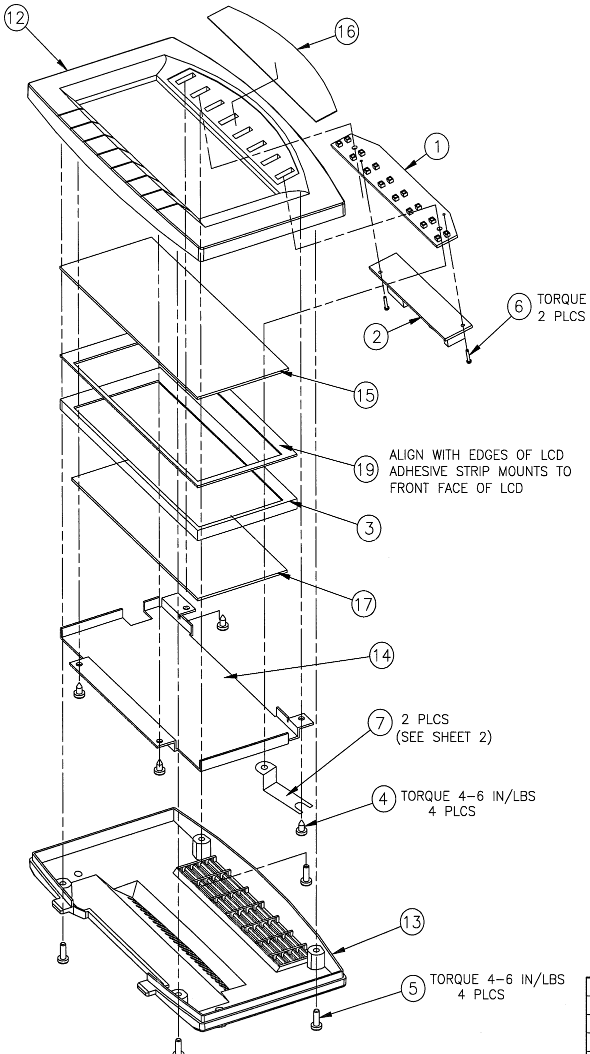
APPROVALS		DATE
DRAWN	AN	9/8/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

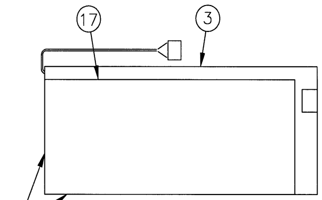
lexicon

TITLE ASSY DWG, MAIN HSG, LARC2

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14231	2
SCALE 1/1		SHEET 2 OF 2	

LEXICON, INC.





DETAIL A (LCD REAR VIEW)

REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG PARTS (4) & (7) PER ECO #000211-00	AN 2/15/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	CORRECT POSITION OF (7) PER ECO #000331-00, ADD (19) PER ECO #000719-00	AN 7/20/00 NB 7/28/00	CW 8/8/00 JW 8/9/00

NOTES

1. SEE SHEET 2 FOR PARTS LIST.
2. APPLY GASKET (17) AS SHOWN ON DETAIL A.

DOCUMENT CONTROL BLOCK

DOC. #	DESCRIPTION	REV.
080-14232	ASSY DWG, DSPLY HSG SHT 1 OF 2	2
080-14232	ASSY DWG, DSPLY HSG SHT 2 OF 2	2

	LARC2
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 14232-21

APPROVALS		DATE
DRAWN	JAM	9/8/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

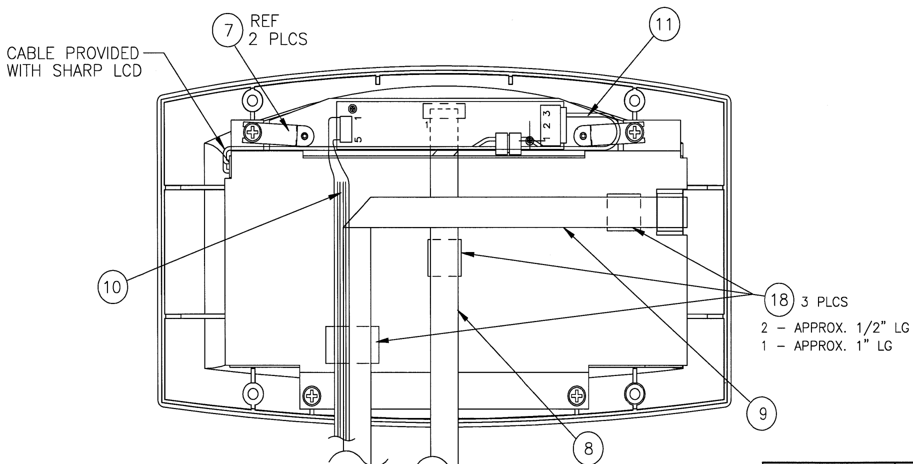
lexicon

TITLE ASSY DWG, DSPLY HSG, LARC2, SHARP

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14232	2
SCALE N/A		SHEET 1 OF 2	

LEXICON, INC.

ITEM #	PART #	DESCRIPTION	QTY	WHERE USED
1.	023-14024	PL, METER BD ASSY	1	
2.	380-13931	DC-AC INV, 2W OUT	1	
3.	430-13934	DISP, LCD, 640X240 DOTS, COLOR	1	
4.	641-01715	SCRW, TAP, AB, 6X3/8, PNH, PH, ZN	4	BRACKET TO HOUSING
5.	640-01716	SCRW, 6-32X3/8, PNH, PH, ZN	4	HOUSING REAR TO FRONT
6.	640-14037	SCRW, 0-80X1/4, PNH, PH, ZN	2	INVERTER TO METER BD
7.	701-14447	CLIP, .78L X .28W X .28H, .100/.156	2	METER BD TO HSG
8.	680-14235	CABLE, FFC, 20CX.5MM, 7.5"	1	METER BD TO MAIN BD
9.	680-14236	CABLE, FFC, 20CX.5MM, 12.5", FOLD	1	LCD TO MAIN BD
10.	680-14238	CABLE, HSG/HSG, 5C/6C, 8.5"	1	INVERTER TO MAIN BD
11.	680-14240	CABLE, CONN/HSG, 2C, 2.5"	1	LCD TO INVERTER
12.	700-14212	HOUSING, DSPLY, FRONT	1	
13.	700-14213	HOUSING, DSPLY, REAR	1	
14.	701-14216	BRACKET, LCD, SHARP	1	
15.	703-14207	LENS, LCD	1	
16.	703-14221	OVLY, METER BRIDGE	1	
17.	720-14224	GASKET, LCD, SHARP	1	
18.	720-10158	TAPE, FOAM, DBL-STK, .5WX.025 THK	2"	TAPE CABLES TO BRACKET
19.	720-14520	SPCR, PVC, ~6.8X3.0X.02", BLK, ADH	1	BETWEEN LCD & LENS



REVISIONS

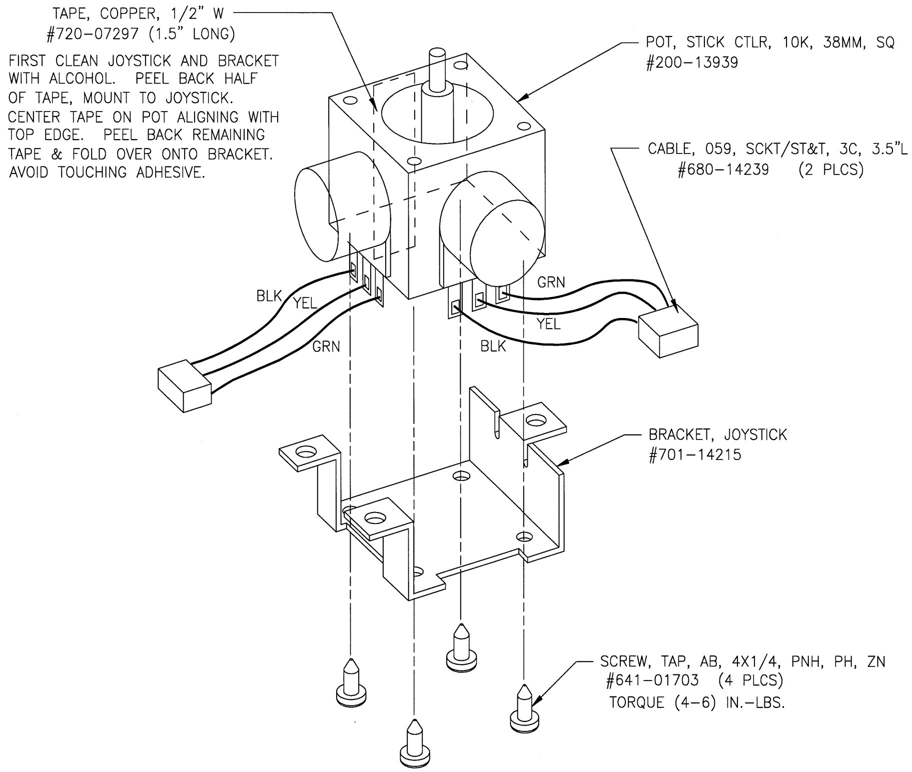
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG PARTS (4) & (7), QTY (18) PER ECO #000211-00	AN 2/11/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	REPOSITION (10) & (18) PER ECO #000331-00, ADD (19) PER ECO #000719-00	AN 7/24/00 NB 7/28/00	CW 8/8/00 JW 8/9/00

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM'S: 022-14027 022-14028

NEXT ASSY	USED ON LARC2	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°	ACAD REL 13 FILE NAME 14232-22	lexicon	
APPLICATION		MATERIAL	APPROVALS / DATE	TITLE ASSY DWG, DSPLY HSG, LARC2, SHARP	
		FINISH	DRAWN AN 9/17/99		
			CHECKED NB 9/29/99	SIZE B / FSCM NO. / DWG. NO. 080-14232	REV. 2
			Q.C. CW 11/1/99		
		DO NOT SCALE DRAWING	ISSUED PJM 11/2/99	SCALE N/A	SHEET 2 OF 2

LEXICON, INC.



REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CLARIFY MTG OF COPPER TAPE PER DCR #000906-00	AN 9/18/00 RL 9/20/00	CW 9/27/00 JW 9/27/00

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM #022-14026

LARC2	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 14233-1

APPROVALS		DATE
DRAWN	JAM	1/27/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

lexicon

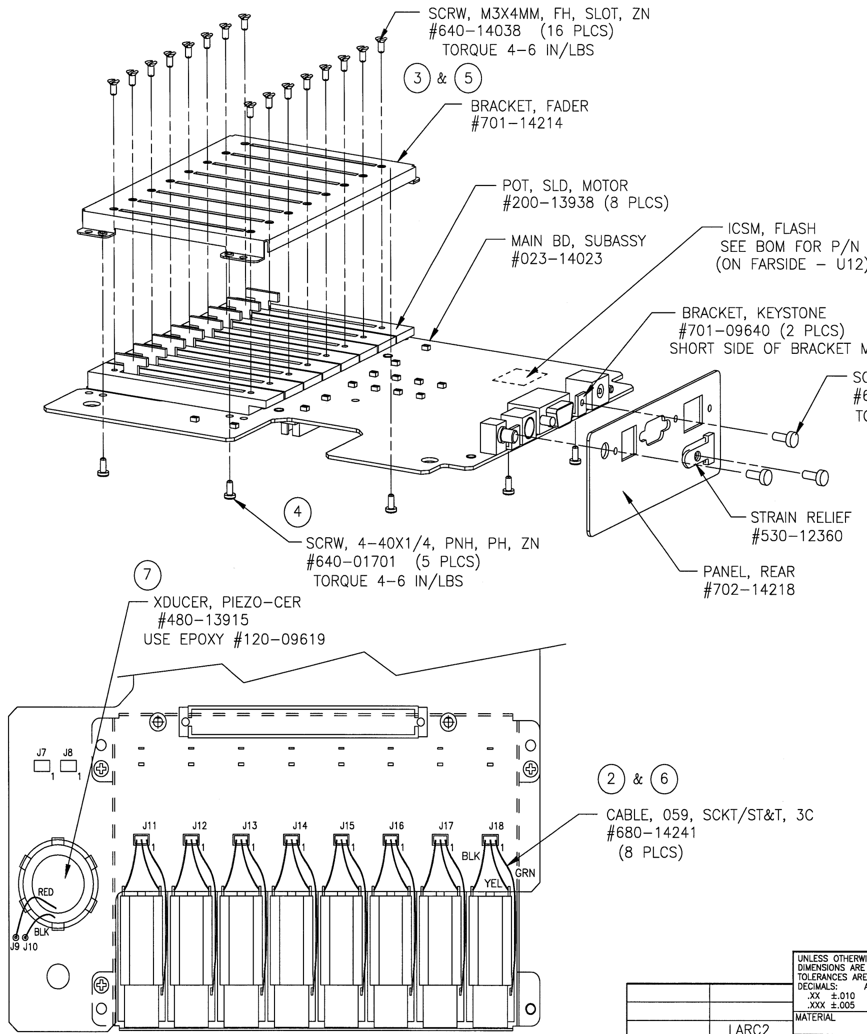
TITLE ASSY DWG, JOYSTICK, LARC2

SIZE	FSCM NO.	DWG. NO.	REV.
C		080-14233	1

SCALE N/A SHEET 1 OF 1

LEXICON, INC.

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG SCRW DESC. (#640-14038) PER ECO #000411-00, ADD XDUCER ASSY INSTR. (NOTE 7) PER ECO #000613-00	AN 7/20/00 NB 7/20/00	CW 7/20/00 ECM 7/20/00
2	REV NOTE 7: ADD SOLDER PADS PER ECO #000802-00	AN 8/3/00 CLC 8/3/00	CW 8/3/00 ECM 8/3/00



ASSEMBLY NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM #023-14023.
2. SOLDER CABLES TO THE 8 POTS (P/N 200-13938)
3. ASSEMBLE POT'S TO THE BRACKET WITH M3 SCREWS, AND LEAVE SCREWS LOOSE.
4. ASSEMBLE THE BRACKET (WITH ATTACHED POTS) TO THE PCB WITH 4-40 SCREWS. MAKE SURE POT CONTACTS HAVE ENTERED ALL CORRESPONDING PCB HOLES AND TIGHTEN 4-40 SCREWS.
5. CENTER POT TANGS IN BRACKET SLOTS AND TIGHTEN M3 SCREWS.
6. SOLDER POT CONTACTS TO THE PCB. PLUG CABLES INTO THEIR RESPECTIVE SOCKETS (J6 THRU J13).
7. TRANSDUCER ASSY INSTRUCTIONS:
   - A. WIPE MATING SURFACES WITH ISO-ALCOHOL OR EQUIV.
   - B. MIX A DOLLOP OF 5-MIN. EPOXY (P/N 120-09619 OR EQUIV.)
   - C. APPLY AN EVEN, THIN LAYER OF EPOXY TO THE TRANSDUCER.
   - D. PLACE THE TRANSDUCER WITHIN THE SILKSCREENED RING ON THE PCB.
   - E. GENTLY PRESS TRANSDUCER ONTO THE PCB. DO NOT CLEAN OFF THE EXCESS.
   - F. AFTER THE EPOXY HAS CURED, SOLDER THE TRANSDUCER TO THE 6 PADS PROVIDED. SOLDER THE PADS ALTERNATELY ACROSS FROM EACH OTHER TO MINIMIZE OVERHEATING.
   - G. SOLDER LEADS TO J9, J10.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°	ACAD REL 13 FILE NAME 14234-2
MATERIAL	DRAWN AN 10/25/99
FINISH	CHECKED NB 9/29/99
	Q.C. CW 11/1/99
DO NOT SCALE DRAWING	ISSUED PJM 11/2/99

NEXT ASSY	USED ON
	LARC2
APPLICATION	

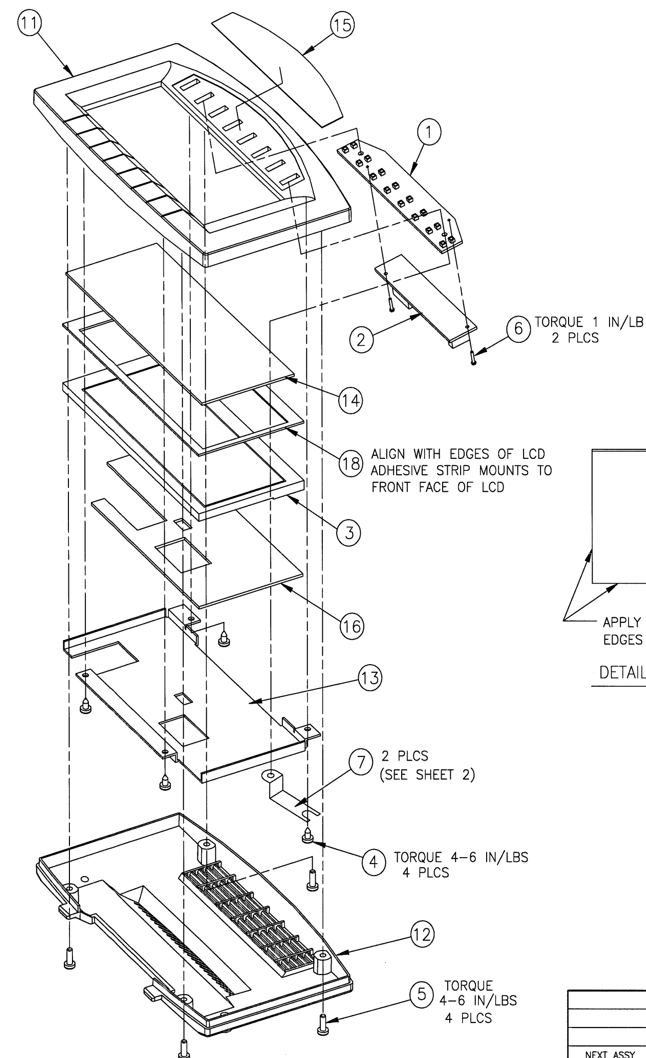
lexicon

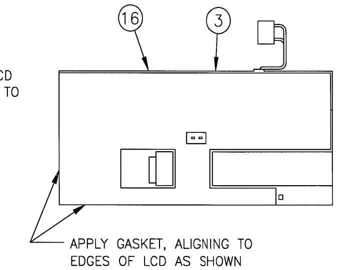
TITLE: ASSY DWG, MECH, MAIN BD, LARC2

SIZE: B | FSCM NO. | DWG. NO.: 080-14234 | REV.: 2

SCALE: N/A | SHEET 1 OF 1

LEXICON, INC.





DETAIL A (LCD REAR VIEW)

REVISIONS			
REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG PARTS (4) & (7) PER ECO #000211-00	AN 2/15/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	CORRECT POSITION OF (7) PER ECO #000331-00, ADD (18) PER ECO #000719-00	AN 7/20/00 NB 7/28/00	CW 8/8/00 JW 8/9/00

NOTES

1. SEE SHEET 2 FOR PARTS LIST.
2. APPLY GASKET (16) AS SHOWN ON DETAIL A.

DOCUMENT CONTROL BLOCK

DOC. #	DESCRIPTION	REV.
080-14242	ASSY DWG, DSPLY HSG SHT 1 OF 2	2
080-14242	ASSY DWG, DSPLY HSG SHT 2 OF 2	2

NEXT ASSY	
USED ON	LARC2
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 14242-21

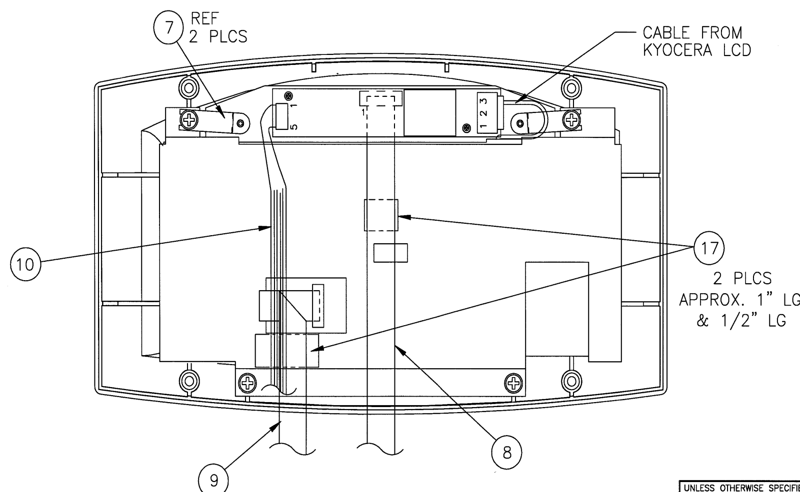
APPROVALS		DATE
DRAWN	JAM	11/9/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

lexicon

TITLE ASSY DWG, DSPLY HSG, LARC2, KYO

SIZE B | FSCM NO. | DWG. NO. 080-14242 | REV. 2
SCALE N/A | SHEET 1 OF 2

ITEM #	PART #	DESCRIPTION	QTY	WHERE USED
1.	023-14024	PL, METER BD ASSY	1	
2.	380-13931	DC-AC INV, 2W OUT	1	
3.	430-14034	DISP, LCD, 640X240 DOTS, COLOR	1	
4.	641-01715	SCRW, TAP, AB, 6X3/8, PNH, PH, ZN	4	BRACKET TO HOUSING
5.	640-01716	SCRW, 6-32X3/8, PNH, PH, ZN	4	HOUSING REAR TO FRONT
6.	640-14037	SCRW, 0-80X1/4, PNH, PH, ZN	2	INVERTER TO METER BD
7.	701-14447	CLIP, .78L X .28W X.26H, .100/.156	2	METER BD TO HSG
8.	680-14235	CABLE, FFC, 20CX.5MM, 7.5"	1	METER BD TO MAIN BD
9.	680-14237	CABLE, FFC, 18CX.5MM, 5.7", FOLD	1	LCD TO MAIN BD
10.	680-14238	CABLE, HSG/HSG, 5C/6C, 8.5"	1	INVERTER TO MAIN BD
11.	700-14212	HOUSING, DSPLY, FRONT	1	
12.	700-14213	HOUSING, DSPLY, REAR	1	
13.	701-14217	BRACKET, LCD, KYOCERA	1	
14.	703-14207	LENS, LCD	1	
15.	703-14221	OVLY, METER BRIDGE	1	
16.	720-14225	GASKET, LCD, KYOCERA	1	
17.	720-10158	TAPE, FOAM, DBL-STK, .5WX .025 THK	1.5"	TAPE CABLES TO BRACKET
18.	720-14520	SPCR, PVC, ~6.8X3.0X.02", BLK, ADH	1	BETWEEN LCD & LENS



REVISIONS

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG PARTS (4) & (7), QTY (17) PER ECO #000211-00	AN 2/11/00 NB 2/25/00	CW 3/1/00 PJM 3/1/00
2	REPOSITION (10) & (17) PER ECO #000331-00, ADD (18) PER ECO #000719-00	AN 7/24/00 NB 7/28/00	CW 8/8/00 JW 8/9/00

NOTES

1. PART NUMBER LISTING IS FOR REFERENCE ONLY & DOES NOT SUPERSEDE BOM'S: 022-14027 022-14029

	LARC2	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°
MATERIAL
FINISH
DO NOT SCALE DRAWING

ACAD REL 13 FILE NAME 14242-22

APPROVALS		DATE
DRAWN	AN	9/16/99
CHECKED	NB	9/29/99
Q.C.	CW	11/1/99
ISSUED	PJM	11/2/99

lexicon

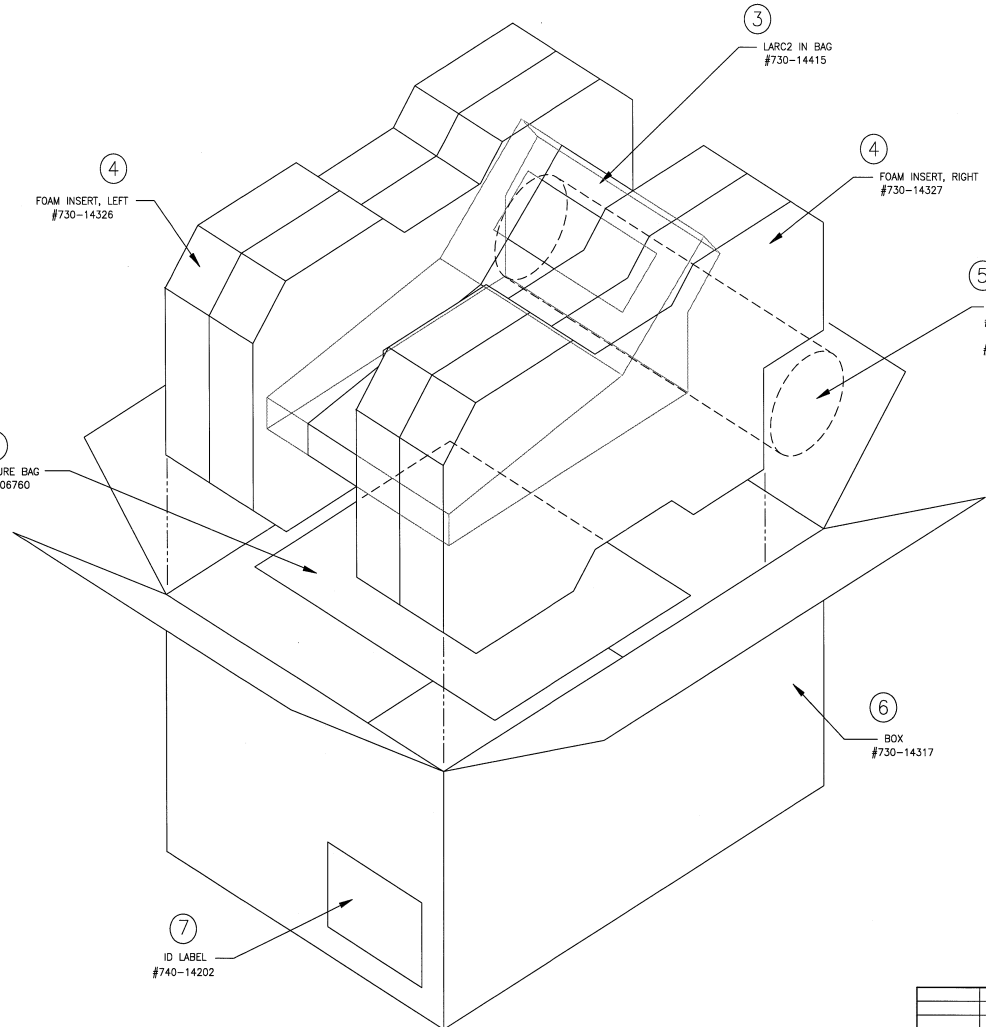
TITLE ASSY DWG, DSPLY HSG, LARC2, KYO

SIZE	FSCM NO.	DWG. NO.	REV.
B		080-14242	2

SCALE 1/1 SHEET 2 OF 2

LEXICON, INC.

REV.	DESCRIPTION	DWR/CHKD	Q.C./AUTH
1	CHG BAG P/N'S, REVISE NOTES PER ECO #000223-00	AN 3/2/00 NB 3/3/00	CW 3/3/00 PJM 3/3/00
2	ADD FERRITE TO CABLE PER ECO #000331-00	AN 7/20/00 NB 7/28/00	CW 8/8/00 JW 8/9/00



NOTES

1. PART NUMBERS SHOWN ARE FOR REFERENCE ONLY AND DO NOT SUPERSEDE BOM #020-14020
2. LITERATURE AND OTHER ITEMS SPECIFIED ON BOM ARE TO BE STACKED IN ORDER OF SIZE, WITH SMALLER ITEMS ON TOP, AND PLACED IN BAG. PLACE IN BOTTOM OF THE BOX.
3. PLACE UNIT IN BAG. HEAT SEAL. (NOTE: FADERS SHOULD BE IN THE UP POSITION.)
4. PLACE LEFT AND RIGHT FOAM INSERTS ON UNIT.
5. SNAP THE FERRITE AROUND THE 50' CABLE AT THE END WITH THE FEMALE CONNECTOR. MOUNT AS CLOSE TO THE CONNECTOR AS POSSIBLE.
6. SLIDE THE UNIT INTO THE BOX WITH THE 50' CABLE IN THE BOTTOM OF THE BOX UNDER THE NOTCH AT THE BACK OF THE FOAM INSERTS.
7. CLOSE BOX FLAPS AND TAPE.
8. ADD ID LABEL TO BOX IN SPACE PROVIDED

	LARC2	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS: .XX ±.010 .XXX ±.005 ANGLES: ±1/2°	ACAD REL 13 FILE NAME 14243-2	lexicon	
NEXT ASSY	USED ON	MATERIAL	APPROVALS / DATE	TITLE ASSY DWG, SHIPMENT, LARC2	
APPLICATION		FINISH	DRAWN AN 11/9/99		
		DO NOT SCALE DRAWING	CHECKED NB 11/17/99	SIZE B / FSCM NO. / DWG. NO. 080-14243	REV. 2
			Q.C. CW 12/1/99	SCALE 1/4	SHEET 1 OF 1
			ISSUED PJM 12/2/99		

LEXICON, INC.

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